1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X941 MLB SCHEMATIC

LAST_MODIFICATION=Wed Jan 10 12:58:52 2018

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0010936498	ENGINEERING RELEASED	2018-01-10

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02166	1	SCHEM,MLB,X941	SCH	CRITICAL	SCH
820-00850	1	PCBF,MLB,X941	PCB	CRITICAL	PCB

?

DRAWING TITLE: SCHEM,MLB,X941

Apple Inc.

DRAWING NUMBER: 051-02166 | SIZE: D

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Module Parts

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00456	1	CPU,CFLU,QMT8,ES,D0,2.3,28W,1.05,BGA1528	U0500	CRITICAL	CPU:2.3G
337S00456	1	CPU,CFLU,QMT8,ES,D0,2.3,28W,1.05,BGA1528	U0500	CRITICAL	CPU:2.5G
337S00456	1	CPU,CFLU,QMT8,ES,D0,2.3,28W,1.05,BGA1528	U0500	CRITICAL	CPU:2.6G
998-10522	1	SOCKET,CPU,CFL-U	U0500	CRITICAL	CPU:SOCKET

SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00370	1	POP,SOC,GIBRALTAR+1GB 20NM,M,B0,CSP1406	U3900	CRITICAL	SOC:B0_1G
339S00372	1	POP,SOC,GIBRALTAR+2GB 20NM,M,B0,CSP1406	U3900	CRITICAL	SOC:B0_2G

SOC Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00371	339S00370	SOC:B0_1G	ALL	Hynix 1GB SCK
339S00375	339S00370	SOC:B0_1G	ALL	Micron 1GB ATK
339S00376	339S00370	SOC:B0_1G	ALL	Hynix 1GB ATK
339S00373	339S00372	SOC:B0_2G	ALL	Hynix 2GB SCK
339S00377	339S00372	SOC:B0_2G	ALL	Micron 2GB ATK
339S00378	339S00372	SOC:B0_2G	ALL	Hynix 2GB ATK

BUILD	SOC	SE
P0	100% A06/B06	100% DEV
P1	100% A06/B06	100% DEV
EVT	100% A09/B09	10% DEV 90% PROD
DVT	95% A09/B09 5% A12/B12	5% DEV (W/ A09/B09 SOC) 95% PROD
PVT	100% A12/B12	100% PROD

SE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-11132	1	IC,RTM4,ES2.1,PN80V,DEV,UFLGA64	U5000	CRITICAL	SE:DEV_2017
338S00253	1	IC,RTM4,ES2.1,PN80V,PRD,UFLGA64	U5000	CRITICAL	SE:PROD_2017

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00356	2	IC,TBT,TITAN RIDGE DP,QTZZ,ES2,B0,CSP337	U2800,UB000	CRITICAL	TBT_TR:B0
338S00399	2	IC,TBT,TITAN RIDGE DP,QTZZ,ES2,C0,CSP337	U2800,UB000	CRITICAL	TBT_TR:C0
338S00408	2	IC,TBT,TITAN RIDGE DP,QUJK,QS,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1

ACE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00961	4	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0_BGA
353S01442	4	IC,CD3215,ACE,C00,USB PWRSW,BLNK,NFBGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0_NFBGA

WIRELESS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00458	1	IC,MODULE,HARPOON,ES7.7,LGA385	U3730	CRITICAL	

PMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00267	1	IC,PMU-A,D2449A0C,CALPE,CSP324,&X28X7.32	U7800	CRITICAL	

CHARGER IC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S01525	1	IC,ISL9240HIB0Z,PMU,SUONA,WCSP40,2.1X3.3	U7000	CRITICAL	

AMR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-10581	2	SUBASSY (T&R) PCBA,AMR INTERPOSER,X941	J4800, J4801	CRITICAL	

DRAM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00125	4	IC,SDRAM,LPDDR3-2133,16GBIT,21NM,H,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HY_8G
333S00069	4	IC,SDRAM,LPDDR3-2133,16GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MI_8G
333S00166	4	IC,SDRAM,LPDDR3-2133,16GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SS_8G
333S00126	4	IC,SDRAM,LPDDR3-2133,32GBIT,21NM,H,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HY_16G
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MI_16G
333S00167	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SS_16G

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00324	4	NAND,3DV3,85GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SD_256G
335S00329	4	NAND,3DV3,85GBP,XXX,S4E,170G,T,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:TO_256G
335S00325	4	NAND,3DV3,128GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SD_512G
335S00330	4	NAND,3DV3,128GBP,XXX,S4E,170G,T,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:TO_512G
335S00327	4	NAND,3DV3,256GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SD_1T
335S00321	4	NAND,3DV3,256GBM,S4E,256G,SS,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SS_1T
335S00332	4	NAND,3DV3,256GBP,XXX,S4E,170G,T,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:TO_1T
335S00322	4	NAND,3DV4,512GBM,S4E,256G,SS,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SS_2T
335S00244	4	NAND,3DV3,512GBM,S4E,256G,SS,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SS_2T_DOE
335S00302	4	NAND,3DV3,85GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:SD_256G_DOE
998-11757	4	NAND,3DV3,85GBP,XXX,S4E,170G,T,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	NAND:TO_256G_DOE

NAND Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00302	335S00324	NAND:SD_256G	ALL	SanDisk 256G Old
335S00290	335S00329	NAND:TO_256G	ALL	Toshiba 256G Old
998-12418	335S00329	NAND:TO_256G	ALL	Toshiba 256G Sub 1
998-12419	335S00329	NAND:TO_256G	ALL	Toshiba 256G Sub 2
335S00303	335S00325	NAND:SD_512G	ALL	SanDisk 512G Old
335S00291	335S00330	NAND:TO_512G	ALL	Toshiba 512G Old
998-12420	335S00330	NAND:TO_512G	ALL	Toshiba 512G Sub 1
998-12421	335S00330	NAND:TO_512G	ALL	Toshiba 512G Sub 2
335S00305	335S00327	NAND:SD_1T	ALL	SanDisk 1T Old
335S00293	335S00332	NAND:TO_1T	ALL	Toshiba 1T Old
998-12424	335S00332	NAND:TO_1T	ALL	Toshiba 1T Sub 1
998-12426	335S00332	NAND:TO_1T	ALL	Toshiba 1T Sub 2

Programmables (All Builds)

TBT ROMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	2	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890,UB090	CRITICAL	TBT_ROM:BLANK
341S00931	1	T29,TR1 (V1.1) PROTO-0,X941	U2890	CRITICAL	TBT_LT_ROM:P0
341S00932	1	T29,TR2 (V1.1) PROTO-1,X941	UB090	CRITICAL	TBT_RT_ROM:P0
341S00959	1	T29,TR1 (V5.1) DCB,X941	U2890	CRITICAL	TBT_LT_ROM:DCB
341S00960	1	T29,TR2 (V5.1) DCB,X941	UB090	CRITICAL	TBT_RT_ROM:DCB
341S00967	1	T29,TR1 (V6.52) PROTO-1,X941	U2890	CRITICAL	TBT_LT_ROM:P1
341S00968	1	T29,TR2 (V6.52) PROTO-1,X941	UB090	CRITICAL	TBT_RT_ROM:P1
341S01028	1	T29,TR1 (VXXXX) EVT,X941	U2890	CRITICAL	TBT_LT_ROM:EVT
341S01029	1	T29,TR2 (VXXXX) EVT,X941	UB090	CRITICAL	TBT_RT_ROM:EVT

BT ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00256	1	IC,SPI SERIAL FLASH,2MBIT,1.8V,DFN8	U3750	CRITICAL	BT_ROM:BLANK
341S0965	1	IC,BT SFLASH ROM (V10.53.122) PROTO-0,X1190	U3750	CRITICAL	BT_ROM:P0
341S0965	1	IC,BT SFLASH ROM (V21) PROTO-1,X1190	U3750	CRITICAL	BT_ROM:P1
341S01025	1	IC,BT SFLASH ROM (VXX) EVT,X1190	U3750	CRITICAL	BT_ROM:EVT

BT ROM Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00248	335S00256	BT_ROM:BLANK	U3750	Macronix
335S00255	335S00256	BT_ROM:BLANK	U3750	Adesto

WIFI ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00214	1	IC,EEPROM,SER,UWIRE,16K,1.8V,DFN8	U3710	CRITICAL	WIFI_ROM:BLANK
341S00725	1	IC,WIFI ROM (V01) WW1,X665	U3710	CRITICAL	WIFI_ROM:P0

WIFI ROM Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00216	335S00214	WIFI_ROM:BLANK	U3710	Rohm

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00456	08	CPU
333S00069	01	MEMORY
333S00070	01	MEMORY
333S00125	01	MEMORY
333S00126	01	MEMORY
333S00166	08	MEMORY
333S00167	08	MEMORY
339S00370	09	pSOC
339S00372	09	pSOC
338S00267	08	CALPE
335S00321	10	NAND
335S00322	10	NAND
335S00324	09	NAND
335S00325	09	NAND
335S00327	09	NAND
335S00329	09	NAND

PART#	STRATEGIC VALUE	COMMENT
335S00330	09	NAND
335S00332	09	NAND
338S00410	08	OCARINA
353S01442	05	ACE
338S00408	08	TITAN RIDGE
353S01188	09	DEBUG MUX2
353S01525	06	SUONA
353S00928	06	IMVP8
353S00526	07	TPS62180
353S01077	02	ISL95870HRUZ
353S01629	08	TAS5770L
353S00253	09	SECURE ELEMENT
353S4415	01	BACKLIGHT CONTROLLER
353S01320	08	MIPI SWITCH
358S1163	01	ACCELEROMETER

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BOM Groups

BOM GROUP	BOM OPTIONS
X941_COMMON	SCH,PCB,ALTERNATE,COMMON,X941_COMMON1,X941_COMMON2,X941_COMMON3,X941_PROGPARTS
X941_COMMON1	TBT_TR:C1,ACE:C0_NFMGA,SE:INV_2017,PMGR:38,SYSGET:YS7,TBTURM_SHS,BOARD_ID,BOARD_REV:180,RF_DOE
X941_COMMON2	EEP_ENABLE,XDP:YES,SKIP_5V3V3:AUDIBLE
X941_COMMON3	LOADRC:YES
X941_PROGPARTS	TBT_LT_ROM:EVT,TBT_RT_ROM:EVT,WIFI_ROM:P0,BT_ROM:EVT
X941_DEVEL:ENG	ALTERNATE,ESPI_DBG,DOGLED,SOC_DBG,USBC_DBG,XDP_CONN:YES,WIFI_DBG,SSD_DBG,SDC_FAN,DEBUG_BUTTON,LOADISRS,AP_TEMP:YES,SENSOR:DEV,BOOTCFG0
X941_DEVEL:DVT	ALTERNATE,SOC_DBG,USBC_DBG,XDP_CONN:YES,WIFI_DBG
X941_DEVEL:PVT	ALTERNATE

Variable BOM Groups
Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00187	1	COMMON PARTS,MLB,X941	BASE	CRITICAL	BASE_BOM
985-00366	1	DEV,MLB,X941	DEVEL	CRITICAL	DEVEL_BOM

NAND Configs

BOM GROUP	BOM OPTIONS
NANDCFG:SD_256G	NAND:SD_256G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:TO_256G	NAND:TO_256G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:SD_512G	NAND:SD_512G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:TO_512G	NAND:TO_512G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:SD_1T	NAND:SD_1T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:SS_1T	NAND:SS_1T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:TO_1T	NAND:TO_1T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:SS_2T	NAND:SS_2T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:SS_2T_DOE	NAND:SS_2T_DOE,SOC:B0_2G,NAND_VCC:2.7V
NANDCFG:SD_256G_DOE	NAND:SD_256G_DOE,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:TO_256G_DOE	NAND:TO_256G_DOE,SOC:B0_1G,NAND_VCC:2.5V

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAMCFG:HY_8G	DRAM:HY_8G,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L
DRAMCFG:MI_8G	DRAM:MI_8G,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L
DRAMCFG:SS_8G	DRAM:SS_8G,RAMCFG3_L,RAMCFG2_L,RAMCFG0_L
DRAMCFG:HY_16G	DRAM:HY_16G,RAMCFG4_L,RAMCFG3_L,RAMCFG1_L,RAMCFG0_L
DRAMCFG:MI_16G	DRAM:MI_16G,RAMCFG4_L,RAMCFG3_L,RAMCFG1_L
DRAMCFG:SS_16G	DRAM:SS_16G,RAMCFG3_L,RAMCFG0_L

CPU DRAM CFG Chart

DIE REV	CFG 4
A	0
B	1

VENDOR	CFG 1	CFG 0
HYNIX	0	0
MICRON	0	1
SAMSUNG	1	0
N/A	1	1

SPEED	CFG 3
2133	0
1866	1

CAPACITY	CFG 2
8GB	0
16GB	1

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PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D
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BOARD MECHANICALS

Shield Cans - BOTTOM SIDE

TITAN RIDGE - LEFT (U2800) - 806-12859

SH0418 SM — FENCE-TITAN-RIDGE-X940

TITAN RIDGE - RIGHT (UB000) - 806-12859

SH0420 SM — FENCE-TITAN-RIDGE-X940

LPDDR3 (U2300 ~ U2600) - 806-15451

SH0415 SM — SHLD-MLB-LPDDR3-X940

NAND - BOTTOM SOUTH (U8700) - 806-12858

SH0417 SM — FENCE-MLB-BTM-NAND-X940

NAND - BOTTOM NORTH (U8900) - 806-12858

SH0419 SM — FENCE-MLB-BTM-NAND-X940

Shield Cans - TOP SIDE

SOC (U3900) - 806-12855

SH0412 SM — FENCE-MLB-BTM-H9M-X940

DIPLEXERS - 806-12854

SH0411 SM — SHLD-MLB-DIPLEXERS-X940

NAND - TOP SOUTH (U8600) - 806-12857

SH0416 SM — FENCE-MLB-NAND-TOP-SOUTH-X940

NAND - TOP NORTH (U8800) - 806-12856

SH0413 SM — FENCE-MLB-NAND-TOP-NORTH-X940

CPU SLED (U0500) - 806-12626

ONLY CABLE

SH0423 SM — SLED-METAL-X940

CPU SLED (U0500) - 806-12626

ONLY CABLE

SH0424 SM — SLED-METAL-X940

POGO PINS

LIO and RIO -2X (870-5071)

SH0471 POGO-2.0OD-2.95H-SM SM

SH0472 POGO-2.0OD-2.95H-SM SM

AROUND THE FAN AND CENTER - 8X (870-01518)

SH0463 POGO-2.3OD-4.0H-SM SM

SH0464 POGO-2.3OD-4.0H-SM SM

SH0465 POGO-2.3OD-4.0H-SM SM

SH0466 POGO-2.3OD-4.0H-SM SM

SH0467 POGO-2.3OD-4.0H-SM SM

SH0468 POGO-2.3OD-4.0H-SM SM

SH0469 POGO-2.3OD-4.0H-SM SM

SH0470 POGO-2.3OD-4.0H-SM SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-14839	2	SLED,METAL,MATT NICKEL,X940	SH0423,SH0424		

Cowling Bosses - BOTTOM SIDE

DFR TOUCH CONN (J4402) - 860-00414

SH0425 6.25X3.85R-1.75ID-1.938H-SM

USB-C CONN - LIO (J3300) - 860-00392

SH0445 3.4OD1.75ID-1.12H-SM

SH0446 3.4OD1.75ID-1.12H-SM

DFR DISPLAY CONN (J4401) - 860-00412

SH0426 3.4OD1.75ID-1.7H-SM

SH0427 3.4OD1.75ID-1.7H-SM

IPD CONN (J4501) - 860-00412

SH0428 3.4OD1.75ID-1.7H-SM

SH0429 3.4OD1.75ID-1.7H-SM

KBD CONN (J4500) - 860-00412

SH0430 3.4OD1.75ID-1.7H-SM

SH0431 3.4OD1.75ID-1.7H-SM

USB-C CONN - RIO (JB500) - 860-00392

SH0447 3.4OD1.75ID-1.12H-SM

SH0448 3.4OD1.75ID-1.12H-SM

AUDIO JACK CONN (J6600) - 860-00829

SH0432 2.7X1.8R-1.4ID-1.64H-SM

MESA CONN (J4900) - 860-00829

SH0433 2.7X1.8R-1.4ID-1.64H-SM

Shield CAN Alignment Slots 14X - 998-04440 (1.2mm X 0.4mm)

SH0449 TH-NSP SL-1.2X0.4-1.5X0.7

SH0450 TH-NSP SL-1.2X0.4-1.5X0.7

SH0451 TH-NSP SL-1.2X0.4-1.5X0.7

SH0452 TH-NSP SL-1.2X0.4-1.5X0.7

SH0453 TH-NSP SL-1.2X0.4-1.5X0.7

SH0454 TH-NSP SL-1.2X0.4-1.5X0.7

SH0455 TH-NSP SL-1.2X0.4-1.5X0.7

SH0457 TH-NSP SL-1.2X0.4-1.5X0.7

SH0458 TH-NSP SL-1.2X0.4-1.5X0.7

SH0459 TH-NSP SL-1.2X0.4-1.5X0.7

SH0460 TH-NSP SL-1.2X0.4-1.5X0.7

SH0461 TH-NSP SL-1.2X0.4-1.5X0.7

Thermal Stage Mounting Holes

Plated Through Hole - 3.15mm - APN 998-0845

SH0490 3P9R3P15

Plated Through Hole - 3.6mm - APN 998-03850

SH0491 4.0R3.6-NSP

SH0492 4.0R3.6-NSP

SH0493 4.0R3.6-NSP

TOP Rubber Mount Standoffs - 12X - (860-00430)

SH0400 2.8OD1.2ID-1.435H-SM

SH0401 2.8OD1.2ID-1.435H-SM

SH0402 2.8OD1.2ID-1.435H-SM

SH0403 2.8OD1.2ID-1.435H-SM

SH0404 2.8OD1.2ID-1.435H-SM

SH0405 2.8OD1.2ID-1.435H-SM

SH0406 2.8OD1.2ID-1.435H-SM

SH0407 2.8OD1.2ID-1.435H-SM

SH0408 2.8OD1.2ID-1.435H-SM

SH0409 2.8OD1.2ID-1.435H-SM

SH0410 2.8OD1.2ID-1.435H-SM

SH0436 2.8OD1.2ID-1.435H-SM

Bottom Rubber Mount Standoffs - 1X - (860-00476)

SH0437 2.8OD1.2ID-3.25H-SM

Cowling Bosses - TOP SIDE

eDP CONN (J8500) - 860-00415

SH0421 3.4OD1.75ID-0.844H-SM

SH0422 3.4OD1.75ID-0.844H-SM

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

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PD Parts

Apple Inc.

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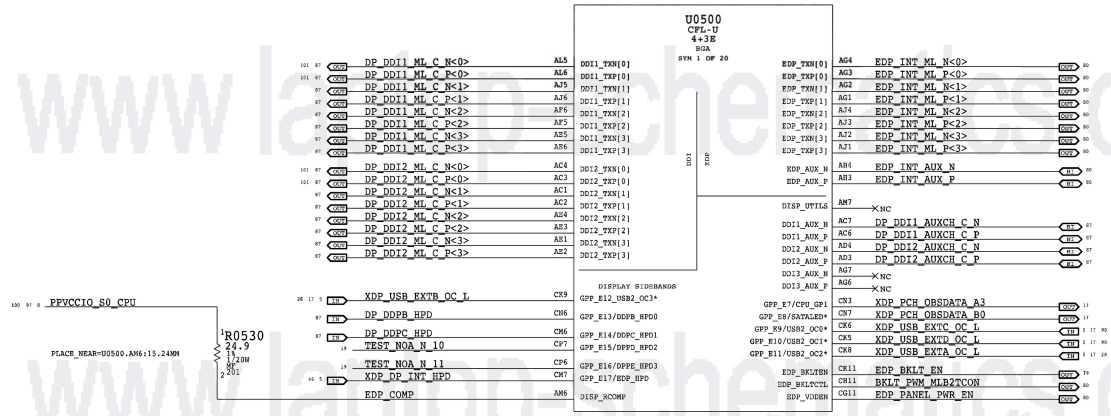

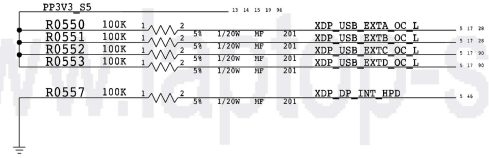

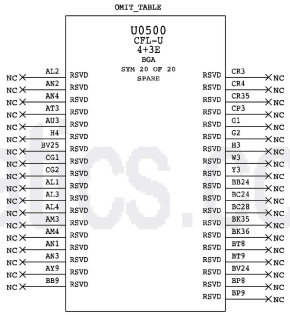

DESIGN: X502/DEV MLB U
LAST CHANGE: Tue Apr 28 20:32:21 2015

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CPU GFX

Apple Inc.

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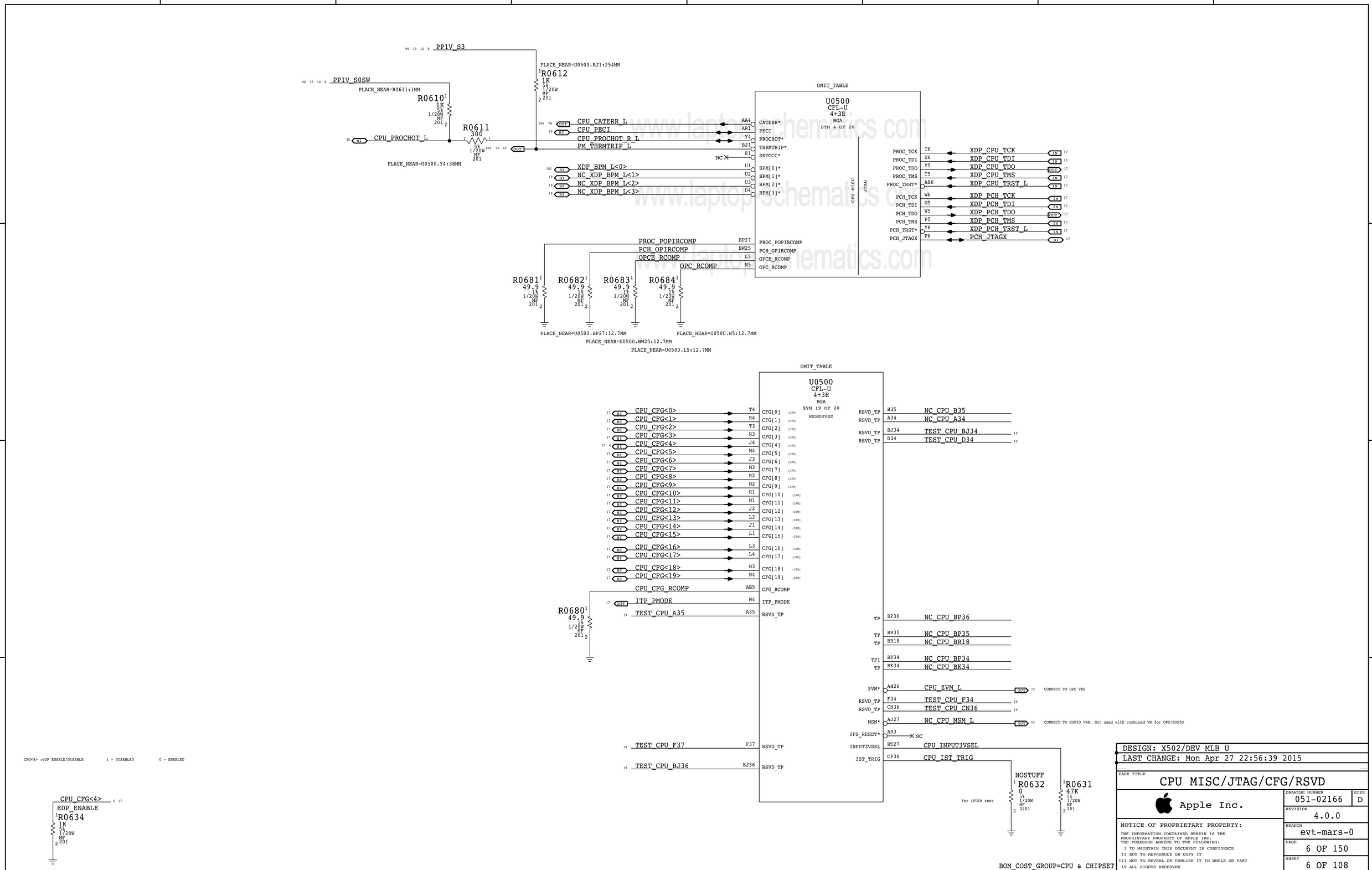
PP1V_S3
PLACE_NEAR=U0500.BJ1:254MM
R0612 1K 5% 1/20W MF 201
PP1V_S0SW
PLACE_NEAR=R0611:1MM
R0610 1K 5% 1/20W MF 201
R0611 300 5% 1/20W MF 201
CPU_PROCHOT_L
PLACE_NEAR=U0500.Y4:38MM
OMIT_TABLE
U0500
CFL-U
4+3E
BGA
SYM 4 OF 20
CPU_CATERR_L
CPU_PECI
CPU_PROCHOT_R_L
PM_THRMTRIP_L
XDP_BPM_L<0>
NC_XDP_BPM_L<1>
NC_XDP_BPM_L<2>
NC_XDP_BPM_L<3>
CPU MISC
JTAG
XDP_CPU_TCK
XDP_CPU_TDI
XDP_CPU_TDO
XDP_CPU_TMS
XDP_CPU_TRST_L
XDP_PCH_TCK
XDP_PCH_TDI
XDP_PCH_TDO
XDP_PCH_TMS
XDP_PCH_TRST_L
PCH_JTAGX
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
R0681 49.9 1% 1/20W MF 201
R0682 49.9 1% 1/20W MF 201
R0683 49.9 1% 1/20W MF 201
R0684 49.9 1% 1/20W MF 201
PLACE_NEAR=U0500.BP27:12.7MM
PLACE_NEAR=U0500.BW25:12.7MM
PLACE_NEAR=U0500.L5:12.7MM
PLACE_NEAR=U0500.N5:12.7MM
OMIT_TABLE
U0500
CFL-U
4+3E
BGA
SYM 19 OF 20
RESERVED
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
CPU_CFG<16>
CPU_CFG<17>
CPU_CFG<18>
CPU_CFG<19>
CPU_CFG_RCOMP
ITP_PMODE
TEST_CPU_A35
TEST_CPU_F37
TEST_CPU_BJ36
NC_CPU_B35
NC_CPU_A34
TEST_CPU_BJ34
TEST_CPU_D34
NC_CPU_BP36
NC_CPU_BP35
NC_CPU_BR18
NC_CPU_BP34
NC_CPU_BK34
CPU_ZVM_L
CONNECT TO OPC VRS
TEST_CPU_F34
TEST_CPU_CN36
NC_CPU_MSM_L
CONNECT TO EOPIO VRS. Not used with combined VR for OPC/EOPIO
CPU_INPUT3VSEL
CPU_IST_TRIG
R0680 49.9 1% 1/20W MF 201
NOSTUFF R0632 0 5% 1/20W MF 0201
For iFDIM test
R0631 47K 5% 1/20W MF 201
CFG<4> :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CPU_CFG<4>
EDP_ENABLE
R0634 1K 5% 1/20W MF 201
BOM_COST_GROUP=CPU & CHIPSET
DESIGN: X502/DEV MLB U
LAST CHANGE: Mon Apr 27 22:56:39 2015
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CPU MISC/JTAG/CFG/RSVD
Apple Inc.
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OMIT_TABLE

U0500
CFL-U
4+3E
BGA
SYM 2 OF 20
LPDDR3 NON-INTERLEAVED0

Signal	Pin	Dir
MEM_A_DQ<0>	A26	BI
MEM_A_DQ<1>	D26	BI
MEM_A_DQ<2>	D28	BI
MEM_A_DQ<3>	C28	BI
MEM_A_DQ<4>	B26	BI
MEM_A_DQ<5>	C26	BI
MEM_A_DQ<6>	B28	BI
MEM_A_DQ<7>	A28	BI
MEM_A_DQ<8>	B30	BI
MEM_A_DQ<9>	D30	BI
MEM_A_DQ<10>	B33	BI
MEM_A_DQ<11>	D32	BI
MEM_A_DQ<12>	A30	BI
MEM_A_DQ<13>	C30	BI
MEM_A_DQ<14>	B32	BI
MEM_A_DQ<15>	C32	BI
MEM_A_DQ<16>	J22	BI
MEM_A_DQ<17>	H25	BI
MEM_A_DQ<18>	G22	BI
MEM_A_DQ<19>	H22	BI
MEM_A_DQ<20>	F25	BI
MEM_A_DQ<21>	J25	BI
MEM_A_DQ<22>	G25	BI
MEM_A_DQ<23>	F22	BI
MEM_A_DQ<24>	D22	BI
MEM_A_DQ<25>	C22	BI
MEM_A_DQ<26>	C24	BI
MEM_A_DQ<27>	D24	BI
MEM_A_DQ<28>	A22	BI
MEM_A_DQ<29>	B22	BI
MEM_A_DQ<30>	A24	BI
MEM_A_DQ<31>	B24	BI
MEM_A_DQ<32>	H37	BI
MEM_A_DQ<33>	H34	BI
MEM_A_DQ<34>	K34	BI
MEM_A_DQ<35>	K35	BI
MEM_A_DQ<36>	H36	BI
MEM_A_DQ<37>	H35	BI
MEM_A_DQ<38>	K36	BI
MEM_A_DQ<39>	K37	BI
MEM_A_DQ<40>	N36	BI
MEM_A_DQ<41>	N34	BI
MEM_A_DQ<42>	R37	BI
MEM_A_DQ<43>	R34	BI
MEM_A_DQ<44>	N37	BI
MEM_A_DQ<45>	N35	BI
MEM_A_DQ<46>	R36	BI
MEM_A_DQ<47>	R35	BI
MEM_A_DQ<48>	G31	BI
MEM_A_DQ<49>	G32	BI
MEM_A_DQ<50>	H29	BI
MEM_A_DQ<51>	H28	BI
MEM_A_DQ<52>	G28	BI
MEM_A_DQ<53>	G29	BI
MEM_A_DQ<54>	H31	BI
MEM_A_DQ<55>	H32	BI
MEM_A_DQ<56>	L31	BI
MEM_A_DQ<57>	L32	BI
MEM_A_DQ<58>	N29	BI
MEM_A_DQ<59>	N28	BI
MEM_A_DQ<60>	L28	BI
MEM_A_DQ<61>	L29	BI
MEM_A_DQ<62>	N31	BI
MEM_A_DQ<63>	N32	BI

Signal	Pin	Dir	Page
DDR0_DQ[0]			
DDR0_DQ[1]			
DDR0_DQ[2]			
DDR0_DQ[3]			
DDR0_DQ[4]			
DDR0_DQ[5]			
DDR0_DQ[6]			
DDR0_DQ[7]			
DDR0_DQ[8]			
DDR0_DQ[9]			
DDR0_DQ[10]			
DDR0_DQ[11]			
DDR0_DQ[12]			
DDR0_DQ[13]			
DDR0_DQ[14]			
DDR0_DQ[15]			
DDR0_DQ[16]			
DDR0_DQ[17]			
DDR0_DQ[18]			
DDR0_DQ[19]			
DDR0_DQ[20]			
DDR0_DQ[21]			
DDR0_DQ[22]			
DDR0_DQ[23]			
DDR0_DQ[24]			
DDR0_DQ[25]			
DDR0_DQ[26]			
DDR0_DQ[27]			
DDR0_DQ[28]			
DDR0_DQ[29]			
DDR0_DQ[30]			
DDR0_DQ[31]			
DDR0_DQ[32]			
DDR0_DQ[33]			
DDR0_DQ[34]			
DDR0_DQ[35]			
DDR0_DQ[36]			
DDR0_DQ[37]			
DDR0_DQ[38]			
DDR0_DQ[39]			
DDR0_DQ[40]			
DDR0_DQ[41]			
DDR0_DQ[42]			
DDR0_DQ[43]			
DDR0_DQ[44]			
DDR0_DQ[45]			
DDR0_DQ[46]			
DDR0_DQ[47]			
DDR0_DQ[48]			
DDR0_DQ[49]			
DDR0_DQ[50]			
DDR0_DQ[51]			
DDR0_DQ[52]			
DDR0_DQ[53]			
DDR0_DQ[54]			
DDR0_DQ[55]			
DDR0_DQ[56]			
DDR0_DQ[57]			
DDR0_DQ[58]			
DDR0_DQ[59]			
DDR0_DQ[60]			
DDR0_DQ[61]			
DDR0_DQ[62]			
DDR0_DQ[63]			

Signal	Pin	Dir	Page
DDR0_CKP[0]	V31		
DDR0_CKN[0]	V32		
DDR0_CKP[1]	T31		
DDR0_CKN[1]	T32		
DDR0_CKE[0]	U36		
DDR0_CKE[1]	U37		
DDR0_CKE[2]	U34		
DDR0_CKE[3]	U35		
DDR0_CS*[0]	AE32		
DDR0_CS*[1]	AF32		
DDR0_ODT[0]	AE31		
NC/DDR0_ODT[1]	AF31	NC	
DDR0_CAA[0]	AB35		
DDR0_CAA[1]	W36		
DDR0_CAA[2]	AA37		
DDR0_CAA[3]	AB34		
DDR0_CAA[4]	AA36		
DDR0_CAA[5]	V34		
DDR0_CAA[6]	AA34		
DDR0_CAA[7]	W34		
DDR0_CAA[8]	V35		
DDR0_CAA[9]	W35		
DDR0_CAB[0]	AC32		
DDR0_CAB[1]	AB32		
DDR0_CAB[2]	AC31		
DDR0_CAB[3]	Y32		
DDR0_CAB[4]	W32		
DDR0_CAB[5]	AC34		
DDR0_CAB[6]	AB31		
DDR0_CAB[7]	Y31		
DDR0_CAB[8]	AC36		
DDR0_CAB[9]	AC37		
DDR0_DQSN[0]	C27		
DDR0_DQSN[1]	D31		
DDR0_DQSN[2]	H24		
DDR0_DQSN[3]	C23		
DDR0_DQSN[4]	J35		
DDR0_DQSN[5]	P34		
DDR0_DQSN[6]	G30		
DDR0_DQSN[7]	L30		
DDR0_DQSP[0]	D27		
DDR0_DQSP[1]	C31		
DDR0_DQSP[2]	G24		
DDR0_DQSP[3]	D23		
DDR0_DQSP[4]	J34		
DDR0_DQSP[5]	P35		
DDR0_DQSP[6]	H30		
DDR0_DQSP[7]	N30		
NC/DDR0_ALERT_L	W37	NC	
NC/DDR0_PAR	W31	NC	
NC/DDR0_MA[3]	AC35	NC	
NC/DDR0_MA[4]	AA35	NC	
DDR_VREF_CA	F36		
DDR0_VREF_DQ[0]	D35		
DDR0_VREF_DQ[1]	D37	NC	
DDR1_VREF_DQ	E36		
DDR_VTT_CNTL	C35		

Signal	Pin	Dir	Page
MEM_A_CLK_P<0>		OUT	21 25
MEM_A_CLK_N<0>		OUT	21 25
MEM_A_CLK_P<1>		OUT	22 25
MEM_A_CLK_N<1>		OUT	22 25
MEM_A_CKE<0>		OUT	21 25
MEM_A_CKE<1>		OUT	21 25
MEM_A_CKE<2>		OUT	22 25
MEM_A_CKE<3>		OUT	22 25
MEM_A_CS_L<0>		OUT	21 22 25
MEM_A_CS_L<1>		OUT	21 22 25
MEM_A_ODT<0>		OUT	21 22 25
MEM_A_CAA<0>		OUT	21 25
MEM_A_CAA<1>		OUT	21 25
MEM_A_CAA<2>		OUT	21 25
MEM_A_CAA<3>		OUT	21 25
MEM_A_CAA<4>		OUT	21 25
MEM_A_CAA<5>		OUT	21 25
MEM_A_CAA<6>		OUT	21 25
MEM_A_CAA<7>		OUT	21 25
MEM_A_CAA<8>		OUT	21 25
MEM_A_CAA<9>		OUT	21 25
MEM_A_CAB<0>		OUT	22 25
MEM_A_CAB<1>		OUT	22 25
MEM_A_CAB<2>		OUT	22 25
MEM_A_CAB<3>		OUT	22 25
MEM_A_CAB<4>		OUT	22 25
MEM_A_CAB<5>		OUT	22 25
MEM_A_CAB<6>		OUT	22 25
MEM_A_CAB<7>		OUT	22 25
MEM_A_CAB<8>		OUT	22 25
MEM_A_CAB<9>		OUT	22 25
MEM_A_DQS_N<0>		BI	99
MEM_A_DQS_N<1>		BI	99
MEM_A_DQS_N<2>		BI	99
MEM_A_DQS_N<3>		BI	99
MEM_A_DQS_N<4>		BI	99
MEM_A_DQS_N<5>		BI	99
MEM_A_DQS_N<6>		BI	99
MEM_A_DQS_N<7>		BI	99
MEM_A_DQS_P<0>		BI	99
MEM_A_DQS_P<1>		BI	99
MEM_A_DQS_P<2>		BI	99
MEM_A_DQS_P<3>		BI	99
MEM_A_DQS_P<4>		BI	99
MEM_A_DQS_P<5>		BI	99
MEM_A_DQS_P<6>		BI	99
MEM_A_DQS_P<7>		BI	99
CPU_DIMM_VREFCA		OUT	20
CPU_DIMMA_VREFDQ		OUT	20
CPU_DIMMB_VREFDQ		OUT	20
PM_MEMVTT_EN		OUT	77

OMIT_TABLE

U0500
CFL-U
4+3E
BGA
SYM 3 OF 20
LPDDR3 NON-INTERLEAVED

Signal	Pin	Dir
MEM_B_DQ<0>	AN35	BI
MEM_B_DQ<1>	AN34	BI
MEM_B_DQ<2>	AR35	BI
MEM_B_DQ<3>	AR34	BI
MEM_B_DQ<4>	AN37	BI
MEM_B_DQ<5>	AN36	BI
MEM_B_DQ<6>	AR36	BI
MEM_B_DQ<7>	AR37	BI
MEM_B_DQ<8>	AU35	BI
MEM_B_DQ<9>	AU34	BI
MEM_B_DQ<10>	AW35	BI
MEM_B_DQ<11>	AW34	BI
MEM_B_DQ<12>	AU37	BI
MEM_B_DQ<13>	AU36	BI
MEM_B_DQ<14>	AW36	BI
MEM_B_DQ<15>	AW37	BI
MEM_B_DQ<16>	AJ29	BI
MEM_B_DQ<17>	AJ30	BI
MEM_B_DQ<18>	AM32	BI
MEM_B_DQ<19>	AM31	BI
MEM_B_DQ<20>	AM30	BI
MEM_B_DQ<21>	AM29	BI
MEM_B_DQ<22>	AJ31	BI
MEM_B_DQ<23>	AJ32	BI
MEM_B_DQ<24>	AR31	BI
MEM_B_DQ<25>	AR32	BI
MEM_B_DQ<26>	AV30	BI
MEM_B_DQ<27>	AV29	BI
MEM_B_DQ<28>	AR30	BI
MEM_B_DQ<29>	AR29	BI
MEM_B_DQ<30>	AV32	BI
MEM_B_DQ<31>	AV31	BI
MEM_B_DQ<32>	BA35	BI
MEM_B_DQ<33>	BA34	BI
MEM_B_DQ<34>	BC35	BI
MEM_B_DQ<35>	BC34	BI
MEM_B_DQ<36>	BA37	BI
MEM_B_DQ<37>	BA36	BI
MEM_B_DQ<38>	BC36	BI
MEM_B_DQ<39>	BC37	BI
MEM_B_DQ<40>	BE35	BI
MEM_B_DQ<41>	BE34	BI
MEM_B_DQ<42>	BG35	BI
MEM_B_DQ<43>	BG34	BI
MEM_B_DQ<44>	BE37	BI
MEM_B_DQ<45>	BE36	BI
MEM_B_DQ<46>	BG36	BI
MEM_B_DQ<47>	BG37	BI
MEM_B_DQ<48>	BA32	BI
MEM_B_DQ<49>	BA31	BI
MEM_B_DQ<50>	BD31	BI
MEM_B_DQ<51>	BD32	BI
MEM_B_DQ<52>	BA30	BI
MEM_B_DQ<53>	BA29	BI
MEM_B_DQ<54>	BD29	BI
MEM_B_DQ<55>	BD30	BI
MEM_B_DQ<56>	BG31	BI
MEM_B_DQ<57>	BG32	BI
MEM_B_DQ<58>	BK32	BI
MEM_B_DQ<59>	BK31	BI
MEM_B_DQ<60>	BG29	BI
MEM_B_DQ<61>	BG30	BI
MEM_B_DQ<62>	BK30	BI
MEM_B_DQ<63>	BK29	BI

Signal	Pin	Dir	Page
DDR1_DQ[0]			
DDR1_DQ[1]			
DDR1_DQ[2]			
DDR1_DQ[3]			
DDR1_DQ[4]			
DDR1_DQ[5]			
DDR1_DQ[6]			
DDR1_DQ[7]			
DDR1_DQ[8]			
DDR1_DQ[9]			
DDR1_DQ[10]			
DDR1_DQ[11]			
DDR1_DQ[12]			
DDR1_DQ[13]			
DDR1_DQ[14]			
DDR1_DQ[15]			
DDR1_DQ[16]			
DDR1_DQ[17]			
DDR1_DQ[18]			
DDR1_DQ[19]			
DDR1_DQ[20]			
DDR1_DQ[21]			
DDR1_DQ[22]			
DDR1_DQ[23]			
DDR1_DQ[24]			
DDR1_DQ[25]			
DDR1_DQ[26]			
DDR1_DQ[27]			
DDR1_DQ[28]			
DDR1_DQ[29]			
DDR1_DQ[30]			
DDR1_DQ[31]			
DDR1_DQ[32]			
DDR1_DQ[33]			
DDR1_DQ[34]			
DDR1_DQ[35]			
DDR1_DQ[36]			
DDR1_DQ[37]			
DDR1_DQ[38]			
DDR1_DQ[39]			
DDR1_DQ[40]			
DDR1_DQ[41]			
DDR1_DQ[42]			
DDR1_DQ[43]			
DDR1_DQ[44]			
DDR1_DQ[45]			
DDR1_DQ[46]			
DDR1_DQ[47]			
DDR1_DQ[48]			
DDR1_DQ[49]			
DDR1_DQ[50]			
DDR1_DQ[51]			
DDR1_DQ[52]			
DDR1_DQ[53]			
DDR1_DQ[54]			
DDR1_DQ[55]			
DDR1_DQ[56]			
DDR1_DQ[57]			
DDR1_DQ[58]			
DDR1_DQ[59]			
DDR1_DQ[60]			
DDR1_DQ[61]			
DDR1_DQ[62]			
DDR1_DQ[63]			

Signal	Pin	Dir	Page
DDR1_CKP[0]	AF29		
DDR1_CKN[0]	AF28		
DDR1_CKP[1]	AE29		
DDR1_CKN[1]	AE28		
DDR1_CKE[0]	T28		
DDR1_CKE[1]	T29		
DDR1_CKE[2]	V28		
DDR1_CKE[3]	V29		
DDR1_CS*[0]	AL37		
DDR1_CS*[1]	AL35		
DDR1_ODT[0]	AL36		
NC/DDR1_ODT[1]	AL34	NC	
DDR1_CAA[0]	AF35		
DDR1_CAA[1]	AB29		
DDR1_CAA[2]	AE37		
DDR1_CAA[3]	AE36		
DDR1_CAA[4]	AC29		
DDR1_CAA[5]	W29		
DDR1_CAA[6]	AB28		
DDR1_CAA[7]	AC28		
DDR1_CAA[8]	W28		
DDR1_CAA[9]	Y28		
DDR1_CAB[0]	AK35		
DDR1_CAB[1]	AK34		
DDR1_CAB[2]	AJ35		
DDR1_CAB[3]	AJ34		
DDR1_CAB[4]	AJ37		
DDR1_CAB[5]	AF34		
DDR1_CAB[6]	AJ36		
DDR1_CAB[7]	AG34		
DDR1_CAB[8]	AG35		
DDR1_CAB[9]	AG36		
DDR1_DQSN[0]	AP35		
DDR1_DQSN[1]	AV34		
DDR1_DQSN[2]	AL31		
DDR1_DQSN[3]	AU31		
DDR1_DQSN[4]	BB35		
DDR1_DQSN[5]	BF34		
DDR1_DQSN[6]	BC31		
DDR1_DQSN[7]	BH31		
DDR1_DQSP[0]	AP34		
DDR1_DQSP[1]	AV35		
DDR1_DQSP[2]	AL30		
DDR1_DQSP[3]	AU30		
DDR1_DQSP[4]	BB34		
DDR1_DQSP[5]	BF35		
DDR1_DQSP[6]	BC30		
DDR1_DQSP[7]	BH30		
NC/DDR1_ALERT_L	Y29	NC	
NC/DDR1_PAR	AE34	NC	
NC/DDR1_MA[3]	AG37	NC	
NC/DDR1_MA[4]	AE35	NC	
DRAM_RESET*	BU31	NC	
DDR_COMP[0]	BN28		
DDR_COMP[1]	BN27		
DDR_COMP[2]	BN29		

Signal	Pin	Dir	Page
MEM_B_CLK_P<0>		OUT	23 25
MEM_B_CLK_N<0>		OUT	23 25
MEM_B_CLK_P<1>		OUT	24 25
MEM_B_CLK_N<1>		OUT	24 25
MEM_B_CKE<0>		OUT	23 25
MEM_B_CKE<1>		OUT	23 25
MEM_B_CKE<2>		OUT	24 25
MEM_B_CKE<3>		OUT	24 25
MEM_B_CS_L<0>		OUT	23 24 25
MEM_B_CS_L<1>		OUT	23 24 25
MEM_B_ODT<0>		OUT	23 24 25
MEM_B_CAA<0>		OUT	23 25
MEM_B_CAA<1>		OUT	23 25
MEM_B_CAA<2>		OUT	23 25
MEM_B_CAA<3>		OUT	23 25
MEM_B_CAA<4>		OUT	23 25
MEM_B_CAA<5>		OUT	23 25
MEM_B_CAA<6>		OUT	23 25
MEM_B_CAA<7>		OUT	23 25
MEM_B_CAA<8>		OUT	23 25
MEM_B_CAA<9>		OUT	23 25
MEM_B_CAB<0>		OUT	24 25
MEM_B_CAB<1>		OUT	24 25
MEM_B_CAB<2>		OUT	24 25
MEM_B_CAB<3>		OUT	24 25
MEM_B_CAB<4>		OUT	24 25
MEM_B_CAB<5>		OUT	24 25
MEM_B_CAB<6>		OUT	24 25
MEM_B_CAB<7>		OUT	24 25
MEM_B_CAB<8>		OUT	24 25
MEM_B_CAB<9>		OUT	24 25
MEM_B_DQS_N<0>		BI	99
MEM_B_DQS_N<1>		BI	99
MEM_B_DQS_N<2>		BI	99
MEM_B_DQS_N<3>		BI	99
MEM_B_DQS_N<4>		BI	99
MEM_B_DQS_N<5>		BI	99
MEM_B_DQS_N<6>		BI	99
MEM_B_DQS_N<7>		BI	99
MEM_B_DQS_P<0>		BI	99
MEM_B_DQS_P<1>		BI	99
MEM_B_DQS_P<2>		BI	99
MEM_B_DQS_P<3>		BI	99
MEM_B_DQS_P<4>		BI	99
MEM_B_DQS_P<5>		BI	99
MEM_B_DQS_P<6>		BI	99
MEM_B_DQS_P<7>		BI	99
CPU_DDR_RCOMP<0>			
CPU_DDR_RCOMP<1>			
CPU_DDR_RCOMP<2>			

R0700 162 1% 1/20W MF 201 — PLACE_NEAR=U0500.BN29:6MM

R0701 80.6 1% 1/20W MF 201 — PLACE_NEAR=U0500.BN27:6MM

R0702 200 1% 1/20W MF 201 — PLACE_NEAR=U0500.BN28:6MM

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J132_GAREN SYNC_DATE=02/03/2017

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CPU LPDDR3 Interface

Apple Inc.

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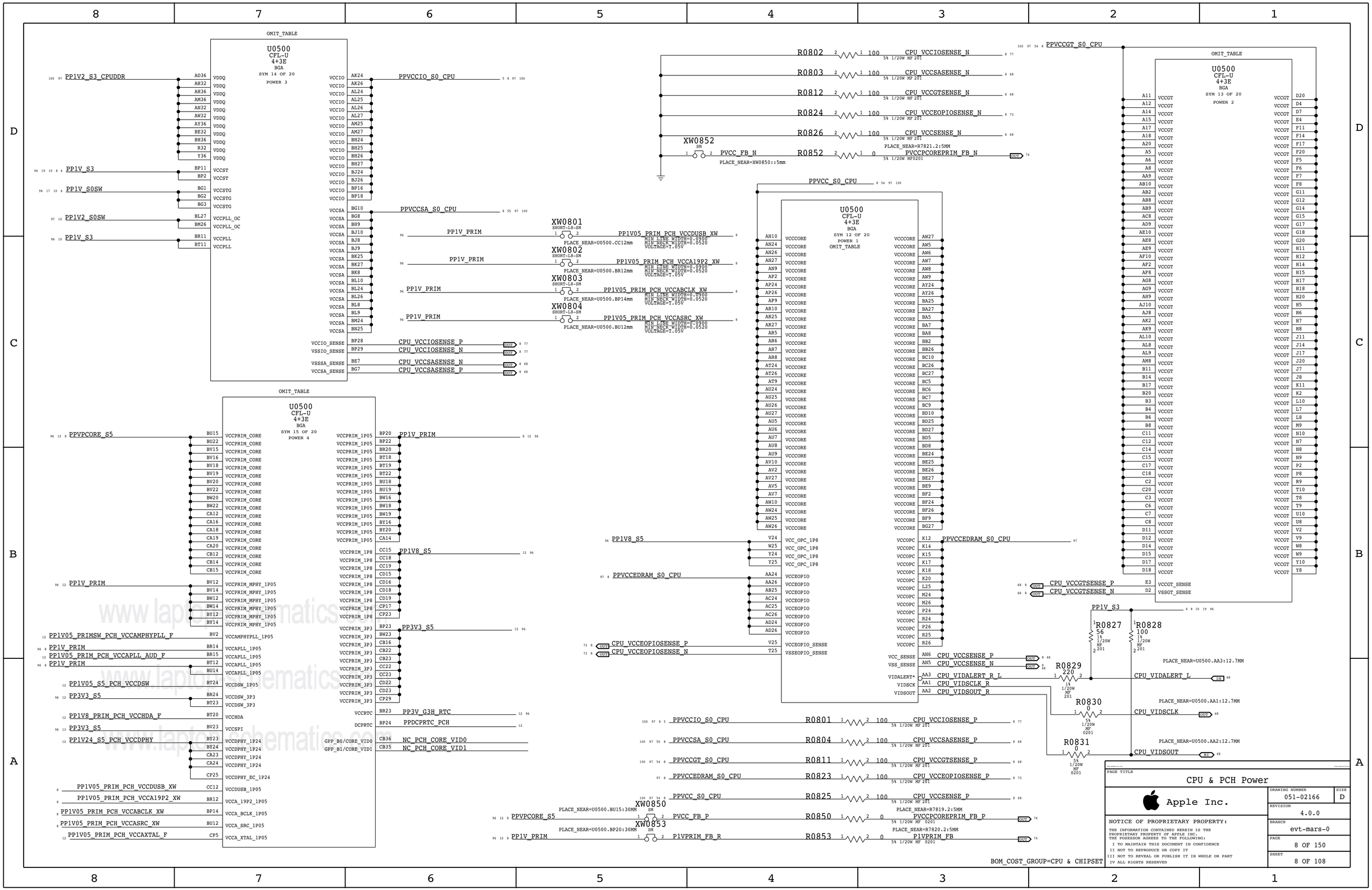
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U0500
CFL-U
4+3E
BGA
SYM 14 OF 20
POWER 3
PP1V2_S3_CPUDDR
PP1V_S3
PP1V_S0SW
PP1V2_S0SW
PP1V_S3
PPVCCIO_S0_CPU
PPVCCSA_S0_CPU
PP1V_PRIM
XW0801
XW0802
XW0803
XW0804
PP1V05_PRIM_PCH_VCCDUSB_XW
PP1V05_PRIM_PCH_VCCA19P2_XW
PP1V05_PRIM_PCH_VCCABCLK_XW
PP1V05_PRIM_PCH_VCCASRC_XW
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N
CPU_VCCSASENSE_N
CPU_VCCSASENSE_P
R0802
R0803
R0812
R0824
R0826
R0852
CPU_VCCIOSENSE_N
CPU_VCCSASENSE_N
CPU_VCCGTSENSE_N
CPU_VCCEOPIOSENSE_N
CPU_VCCSENSE_N
PVCCPCOREPRIM_FB_N
XW0852
PVCC_FB_N
PPVCCGT_S0_CPU
PPVCC_S0_CPU
PPVPCORE_S5
PP1V_PRIM
PP1V8_S5
PP3V3_S5
NC_PCH_CORE_VID0
NC_PCH_CORE_VID1
PP1V8_S5
PPVCCEDRAM_S0_CPU
CPU_VCCEOPIOSENSE_P
CPU_VCCEOPIOSENSE_N
CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
PP1V_S3
R0827
R0828
R0829
R0830
R0831
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0801
R0804
R0811
R0823
R0825
R0850
R0853
CPU_VCCIOSENSE_P
CPU_VCCSASENSE_P
CPU_VCCGTSENSE_P
CPU_VCCEOPIOSENSE_P
CPU_VCCSENSE_P
PVCCPCOREPRIM_FB_N
P1VPRIM_FB
XW0850
XW0853
PVCC_FB_P
P1VPRIM_FB_R
BOM_COST_GROUP=CPU & CHIPSET
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CPU & PCH Power
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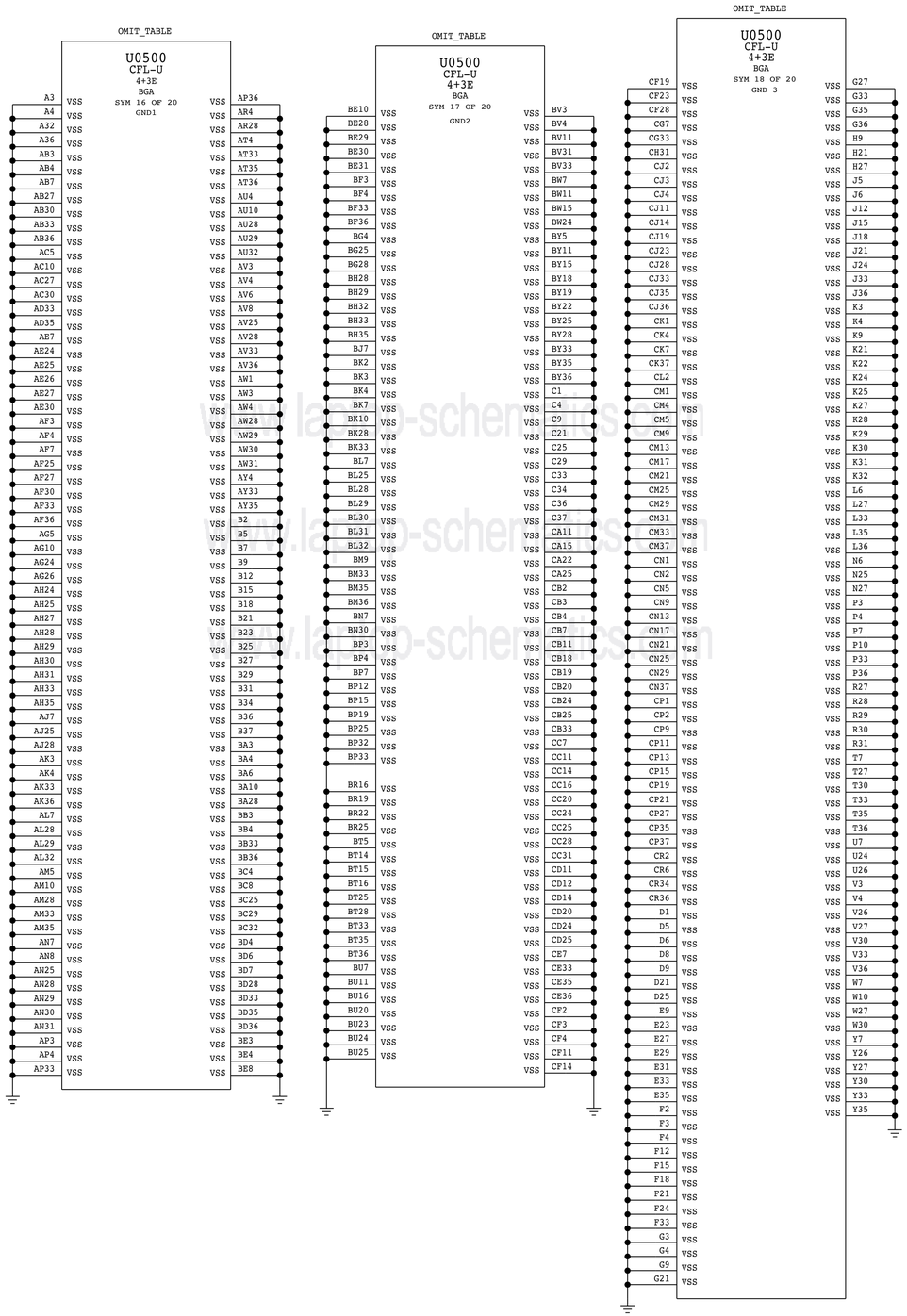

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CPU & PCH Grounds

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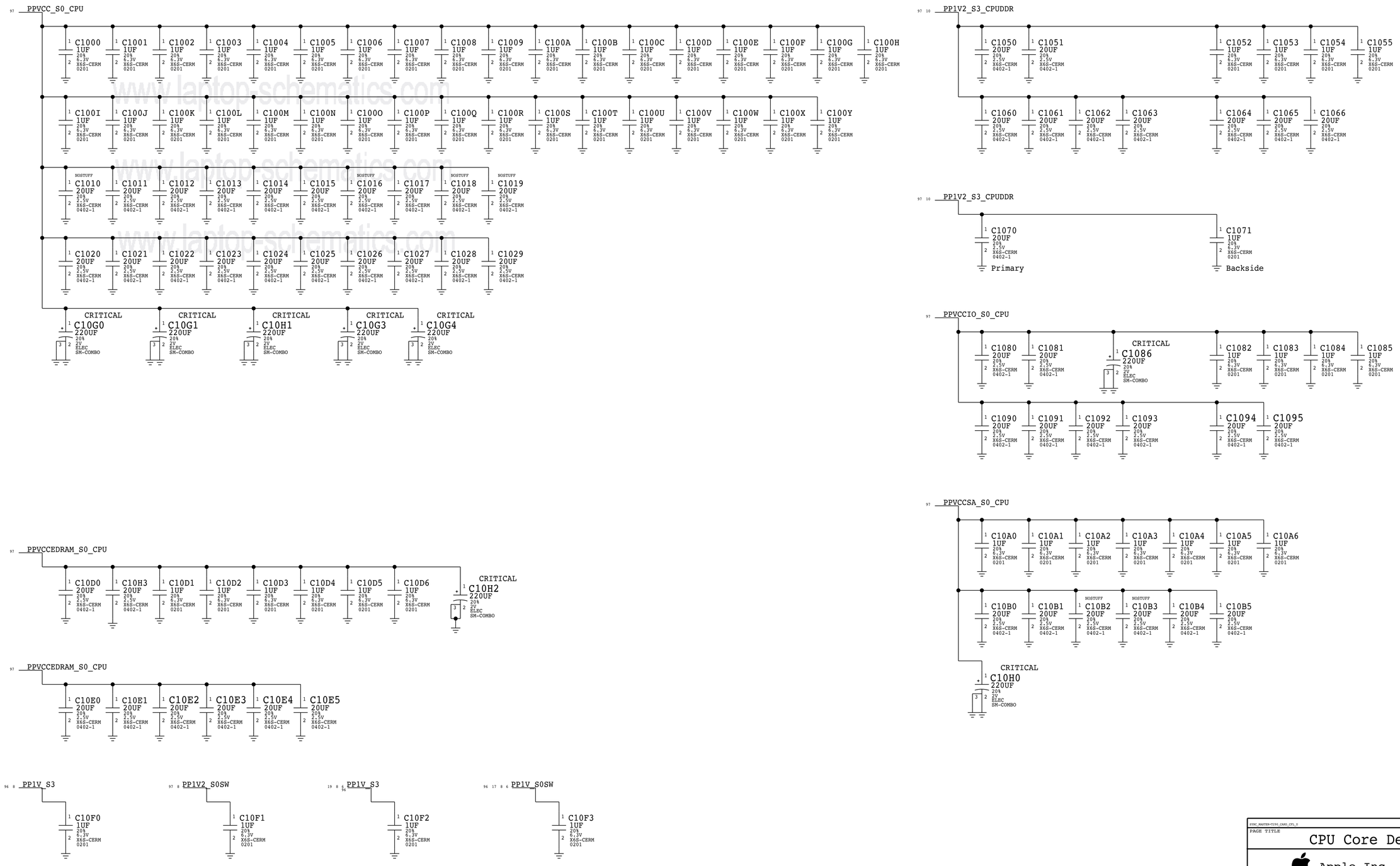

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BOM_COST_GROUP=CPU & CHIPSET

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CPU Core Decoupling

Apple Inc.

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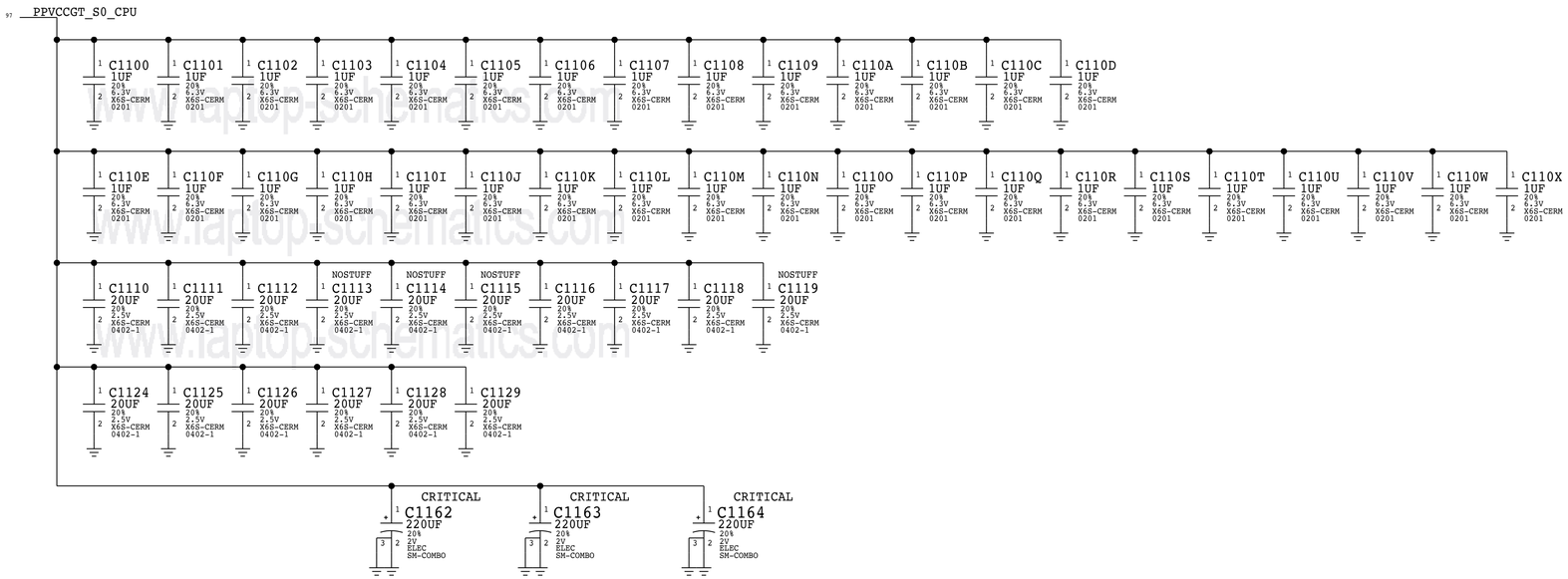

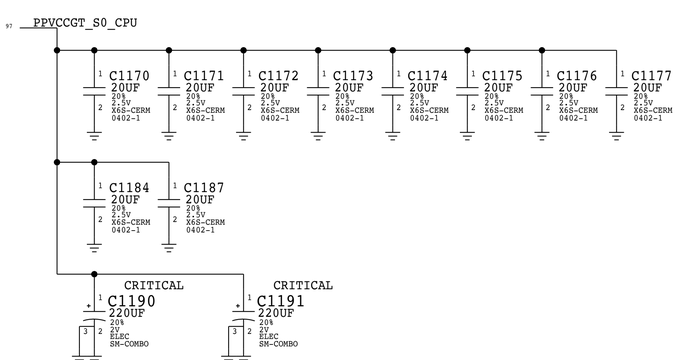

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SYNC_MASTER=T290_CPU SYNC_DATE=07/19/2016

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CPU GT Decoupling

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RAIL SIDE PCH SIDE

PPVPCORE_S5 — NOSTUFF C1200 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.BV18::3MM

PP1V_PRIM — C1201 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.BP20::3MM

PP1V_PRIM — CRITICAL C1203 20UF 20% 6.3V CERM-X5R 0402 — BYPASS=U0500.BV12::12MM

PP1V8_S5 — C1205 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.CP17::3MM; NOSTUFF C1206 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.CP23::3MM

PP3V3_S5 — NOSTUFF C1207 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.CD23::3MM; NOSTUFF C1208 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U0500.CP29::3MM

PP3V3_S5 — NOSTUFF C1221 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.BR24::3MM

PP1V05_S5_PCH_VCCDSW (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.05V) — C1232 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.BT24::3MM

PP3V_G3H_RTC — C1227 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.BR23::3MM; C1228 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U0500.BR23::3MM

PPDCPRTC_PCH (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=3.3V) — C1231 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U0500.BP24::3MM

PP1V24_S5_PCH_VCCDPHY (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.24V) — C1224 4.7UF 20% 6.3V X5R-CERM1 402 — BYPASS=U0500.CP25::3MM

PP1V8_S5 — L1260 220-OHM-0.7A-0.28-OHM 0402-1 U0500.BT20::10mm — PP1V8_PRIM_PCH_VCCHDA_F; PP1V8_PRIM_PCH_VCCHDA_F (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.8V, MAKE_BASE=TRUE)
- C1265 3.0PF ±/-0.1PF 25V NP0-COG 0201
- C1226 2.0PF ±/-0.1PF 25V C0G-CERM 0201 — BYPASS=U0500.BT20::10mm
- C1260 4.7UF 20% 6.3V X5R-CERM1 402 — BYPASS=U0500.BT20::10MM

PP1V_PRIM — L1261 220-OHM-0.7A-0.28-OHM 0402-1 U0500.BR15::3mm — PP1V05_PRIM_PCH_VCCAPLL_AUD_F; PP1V05_PRIM_PCH_VCCAPLL_AUD_F (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- C1267 3.0PF ±/-0.1PF 25V NP0-COG 0201
- C1262 2.0PF ±/-0.1PF 25V C0G-CERM 0201 — BYPASS=U0500.BR15::3mm
- C1261 4.7UF 20% 6.3V X5R-CERM1 402 — BYPASS=U0500.BR15::3MM

PP1V_PRIM — R1250 0 5% 1/16W MF-LF 402 — BYPASS=U0500.BV2::3MM
- CRITICAL C1250 20UF 20% 6.3V CERM-X5R 0402
- CRITICAL C1251 20UF 20% 6.3V CERM-X5R 0402 — BYPASS=U0500.BV2::3MM
- C1252 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.BV2::3MM

PP1V05_PRIMSW_PCH_VCCAMPHYPLL_F; PP1V05_PRIMSW_PCH_VCCAMPHYPLL_F (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.05V, MAKE_BASE=TRUE)

PP1V_PRIM — R1253 0 5% 1/16W MF-LF 402 — BYPASS=U0500.CP5::3MM
- CRITICAL C1253 20UF 20% 6.3V CERM-X5R 0402
- CRITICAL C1254 20UF 20% 6.3V CERM-X5R 0402 — BYPASS=U0500.CP5::3MM
- C1255 1UF 20% 6.3V X6S-CERM 0201 — BYPASS=U0500.CP5::3MM

PP1V05_PRIM_PCH_VCCAXTAL_F; PP1V05_PRIM_PCH_VCCAXTAL_F (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.05V, MAKE_BASE=TRUE)

BOM_COST_GROUP=CPU & CHIPSET

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Apple Inc.	DRAWING NUMBER 051-02166 — SIZE D
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ALL GPP_F* PINS ARE 1.8V ONLY!

OMIT_TABLE

U0500
CFL-U
4+3E
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Signal	Pin	Net
HDA_SYNC/I2S0_SFRM	BN34	NC_PCH_I2S0_SYNC
HDA_BCLK/I2S0_SCLK	BN37	NC_PCH_I2S0_CLK
HDA_SDO/I2S0_TXD	BN36	NC_HDA_SDOUT
HDA_SDI0/I2S0_RXD	BN35	NC_PCH_I2S0_D2R
HDA_SDI1/I2S1_RXD	BL36	NC
HDA_RST*/I2S1_SCLK	BL35	NC_PCH_I2S1_CLK
GPP_D17/DMIC_CLK1	CK25	NC_PCH_GPP_D17
I2S1_SFRM	BL37	NC
I2S1_TXD	BL34	NC
GPP_E18/DPPB_CTRLCLK	CC8	JTAG_TBT_X_TMS (26 13 OUT)
GPP_E19/DPPB_CTRLDATA	CC9	PCH_DDPB_CTRLDATA (19 IN)
GPP_E20/DPPC_CTRLCLK	CH4	JTAG_TBT_T_TMS (88 13 BI)
GPP_E21/DPPC_CTRLDATA	CH3	PCH_DDPC_CTRLDATA (19 IN)
GPP_D13/ISH_UART0_RXD/SMLUBDATA/I2C4B_SDA	CM24	MLB_RAMCFG0 (13)
GPP_D14/ISH_UART0_TXD/SMLUBCLK/I2C4B_SCL	CN23	MLB_RAMCFG1 (13)
GPP_D11	CM22	NC_PCH_GPP_D11
GPP_D12	CP22	PCH_STRP_JTAGODTDIS (13)
GPP_B14/SPKR	CF35	NC_PCH_STRP_TOPBLK_SWP_L
GPP_F0/CNV_PA_BLANKING	CP20	NC_PCH_GPP_F0
GPP_F1	CK19	NC_PCH_GPP_F1
GPP_F2	CG17	NC_PCH_GPP_F2
GPP_F3	CN20	NC_PCH_GPP_F3
GPP_H4/I2C2_SDA	CF27	NC_PCH_I2C_UPC_SDA
GPP_H5/I2C2_SCL	CF29	NC_PCH_I2C_UPC_SCL
GPP_H6/I2C3_SDA	CH27	NC_PCH_GPP_H6
GPP_H7/I2C3_SCL	CH28	NC_PCH_GPP_H7
GPP_H8/I2C4_SDA	CJ30	NC_PCH_GPP_H8
GPP_H9/I2C4_SCL	CJ31	NC_PCH_GPP_H9
GPP_H10/I2C5_SDA/ISH_I2C2_SDA	CJ27	NC_PCH_GPP_H10
GPP_H11/I2C5_SCL/ISH_I2C2_SCL	CJ29	NC_PCH_GPP_H11

Signal	Pin	Net
GPP_F18/EMMC_DATA6	CP18	NC_PCH_GPP_F18
GPP_F19/EMMC_DATA7	CM18	NC_PCH_GPP_F19
GPP_F20/EMMC_RCLK	CM16	NC_PCH_GPP_F20
GPP_F21/EMMC_CLK	CP16	NC_PCH_GPP_F21
GPP_F22/EMMC_RESET*	CN16	NC_PCH_GPP_F22
GPP_F23	CF17	NC_PCH_GPP_F23
GPP_G0/SD_CMD	CH36	TBT_X_CIO_PWR_EN (OUT 13 26 28 29 30)
GPP_G1/SD3_DATA0	CL35	TBT_X_USB_PWR_EN (OUT 13 26 28 29 30)
GPP_A17/SD_VDD1_PWR_EN*/ISH_GP7	BW36	NC_PCH_GPP_A17
GPP_A16/SD_1P8_SEL	BY31	NC_PCH_GPP_A16
SD_1P8_RCOMP	CK33	SD_RCOMP
SD_3P3_RCOMP	CM34	
GPP_F17/EMMC_DATA5	CR18	NC_PCH_GPP_F17
GPP_H12/M2_SKT2/CFG[0]	CR28	JTAG_ISP_TCK (OUT 13 26 88)
GPP_H13/M2_SKT2/CFG[1]	CP28	JTAG_ISP_TDI (OUT 13 26 88)
GPP_H14/M2_SKT2/CFG[2]	CN28	JTAG_ISP_TDO (IN 13 26 88)
GPP_H15/M2_SKT2/CFG[3]	CM28	TBT_POC_RESET (OUT 13 28 90)
GPP_H16/DDPF_CTRLCLK	CR26	NC_PCH_GPP_H16
GPP_H17/DDPF_CTRLDATA	CP26	NC_PCH_DDPF_CTRLDATA
GPP_H18/CPU_C10_GATE*	CN27	CPU_C10_GATE_L (OUT 13 75 77 78)
GPP_H19/TIMESYNC[0]	CM27	WLAN_AUDIO_SYNC (IN 13 35 37)
GPP_H20/IMGCLKOUT[1]	CH25	NC_PCH_GPP_H20
GPP_H21	CF25	PCH_STRP_XTAL_24MHZ (13)
GPP_H22	CN26	NC_PCH_GPP_H22
GPP_H23	CM26	PCH_STRP_SPIROM_SAF (13)

R1370 200 1% 1/20W MF 201 (PLACE_NEAR=U0500.CK33:12.7MM)

OMIT_TABLE

U0500
CFL-U
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Signal	Pin	Net
SPI0_CLK	CH37	TP_SPI_PCHROM_CLK
SPI0_MISO	CF37	NC_SPI_PCHROM_MISO
SPI0_MOSI	CF36	SPI_PCHROM_MOSI (13)
SPI0_IO2	CF34	SPI_PCHROM_IO<2> (17 13)
SPI0_IO3	CG34	SPI_PCHROM_IO<3> (13)
SPI0_CS0*	CG36	TP_SPI_PCHROM_CS_L
SPI0_CS1*	CG35	NC_SPI_CS1_L
SPI0_CS2*	CH34	NC_SPI_CS2_L
GPP_C20/UART2_RXD	CR12	PCH_UART_DEBUG_D2R (103 100 28 13 IN)
GPP_C21/UART2_TXD	CP12	PCH_UART_DEBUG_R2D (103 100 28 13 OUT)
GPP_C22/UART2_RTS*	CN12	NC_PCH_GPP_C22
GPP_C23/UART2_CTS*	CM12	PCH_UART2_CTS_L (13)
GPP_D15/ISH_UART0_RTS*	CM23	MLB_RAMCFG2 (13)
GPP_D16/ISH_UART0_CTS*	CR24	MLB_RAMCFG3 (13)
GPP_D21/SPI1_IO2	CG23	MLB_RAMCFG4 (13)
CL_CLK	CH7	NC
CL_DATA	CH8	NC
CL_RST*	CH9	NC
GPP_A0/RCIN*	BV29	PCH_GPP_A0_PU (13)
GPP_A6/SERIRQ	BV28	NC_PCH_GPP_A6

Signal	Pin	Net
GPP_C0/SMBCLK	CK14	SMBUS_PCH_CLK (OUT 50)
GPP_C1/SMBDATA	CH15	SMBUS_PCH_DATA (BI 50)
GPP_C2/SMBALERT*	CJ15	NC_PCH_STRP_TLSCONF
GPP_C3/SML0CLK	CH14	SML_PCH_0_CLK (OUT 50)
GPP_C4/SML0DATA	CP15	SML_PCH_0_DATA (BI 50)
GPP_C5/SML0ALERT*	CG15	PCH_STRP_ESPI (13)
GPP_C6/SML1CLK	CN15	I2C_SNS1_S0_SCL (OUT 50)
GPP_C7/SML1DATA	CM15	I2C_SNS1_S0_SDA (BI 50)
GPP_B23/SML1ALERT*/PCHHOT*	CC34	NC_PCH_STRP_BSSB_SEL_GPIO
GPP_A1/LAD0/ESPI_IO0	CA29	ESPI_IO_PCH<0> — R1320 20 — ESPI_IO<0> (BI 19 38)
GPP_A2/LAD1/ESPI_IO1	BY29	ESPI_IO_PCH<1> — R1321 20 — ESPI_IO<1> (BI 19 38)
GPP_A3/LAD2/ESPI_IO2	BY27	ESPI_IO_PCH<2> — R1322 20 — ESPI_IO<2> (BI 19 38)
GPP_A4/LAD3/ESPI_IO3	BV27	ESPI_IO_PCH<3> — R1323 20 — ESPI_IO<3> (BI 19 38)
GPP_A5/LFRAME*/ESPI_CS*	CA28	ESPI_CS_L (OUT 19 38)
GPP_A14/SUS_STAT*/ESPI_RESET*	CA27	ESPI_RESET_L (OUT 19 38)
GPP_A9/CLKOUT_LPC0/ESPI_CLK	BV32	ESPI_CLK60M_R — R1327 22 — ESPI_CLK60M (OUT 19 38)
GPP_A10/CLKOUT_LPC1	BV30	NC_PCH_GPP_A10
GPP_A8/CLKRUN*	BY30	NC_PCH_GPP_A8

PP3V3_S5 (8 96)

R1366	100K	5%	1/20W	MF	201	SPI_PCHROM_MOSI	(13)
R1367	100K	5%	1/20W	MF	201	SPI_PCHROM_IO<2>	(13 17)
R1368	100K	5%	1/20W	MF	201	SPI_PCHROM_IO<3>	(13)

PP1V8_S5 (14 15 16 38 96)

R1344	100K	5%	1/20W	MF	201	PCH_GPP_A0_PU	(13)
R1345	1K	5%	1/20W	MF	201	PCH_STRP_ESPI	(13)
R1352	47K	5%	1/20W	MF	201	PCH_UART_DEBUG_D2R	(13 28 100 103)
R1353	47K	5%	1/20W	MF	201	PCH_UART_DEBUG_R2D	(13 28 100 103)
R1363	1K	5%	1/20W	MF	201	PCH_STRP_SPIROM_SAF	(13)
R1365	1K	5%	1/20W	MF	201	PCH_STRP_XTAL_24MHZ	(13)

PP3V3_S5 (5 14 15 19 96)

R1346	100K	5%	1/20W	MF	201	PCH_STRP_JTAGODTDIS	(13)
R1355	10K	5%	1/20W	MF	201	JTAG_TBT_X_TMS	(13 26)
R1356	10K	5%	1/20W	MF	201	JTAG_TBT_T_TMS	(13 88)
R1359	10K	5%	1/20W	MF	201	JTAG_ISP_TDO	(13 26 88)
R1347	100K	5%	1/20W	MF	201	CPU_C10_GATE_L	(13 75 77 78)

Need to Revew
move or remove

PP3V3_TBT_X_S0 (97)

R1357	100K	5%	1/20W	MF	201	NOSTUFF	TBT_X_CIO_PWR_EN (13 26 28 29 30)
R1358	100K	5%	1/20W	MF	201	NOSTUFF	TBT_X_USB_PWR_EN (13 26 28 29 30)

PM_SLP_S3_L (14 16 26 88 100 103)

R1371	100K	5%	1/20W	MF	201		TBT_X_CIO_PWR_EN (13 26 28 29 30)
R1372	100K	5%	1/20W	MF	201		TBT_X_USB_PWR_EN (13 26 28 29 30)

R1360	100K	5%	1/20W	MF	201		JTAG_ISP_TCK (13 26 88)
R1361	100K	5%	1/20W	MF	201		JTAG_ISP_TDI (13 26 88)
R1354	47K	5%	1/20W	MF	201		PCH_UART2_CTS_L (13)
R1362	100K	5%	1/20W	MF	201		TBT_POC_RESET (13 28 90)
R1364	100K	5%	1/20W	MF	201		WLAN_AUDIO_SYNC (13 35 37)

MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 1.8V.

MLB_RAMCFG0 (13)					R1330 1K 5% 1/20W MF 201
MLB_RAMCFG1 (13)				R1331 1K 5% 1/20W MF 201	
MLB_RAMCFG2 (13)			R1332 1K 5% 1/20W MF 201		
MLB_RAMCFG3 (13)		R1333 1K 5% 1/20W MF 201			
MLB_RAMCFG4 (13)	R1334 1K 5% 1/20W MF 201				
	RAMCFG4_L	RAMCFG3_L	RAMCFG2_L	RAMCFG1_L	RAMCFG0_L

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue Feb 2 13:18:21 2016

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PCH Audio/LPC/SPI/SMBus

Apple Inc.

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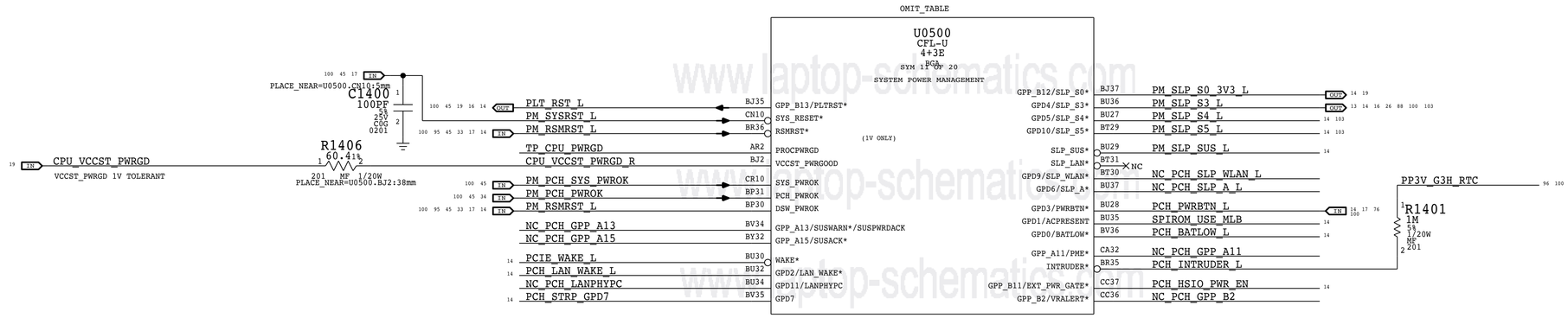

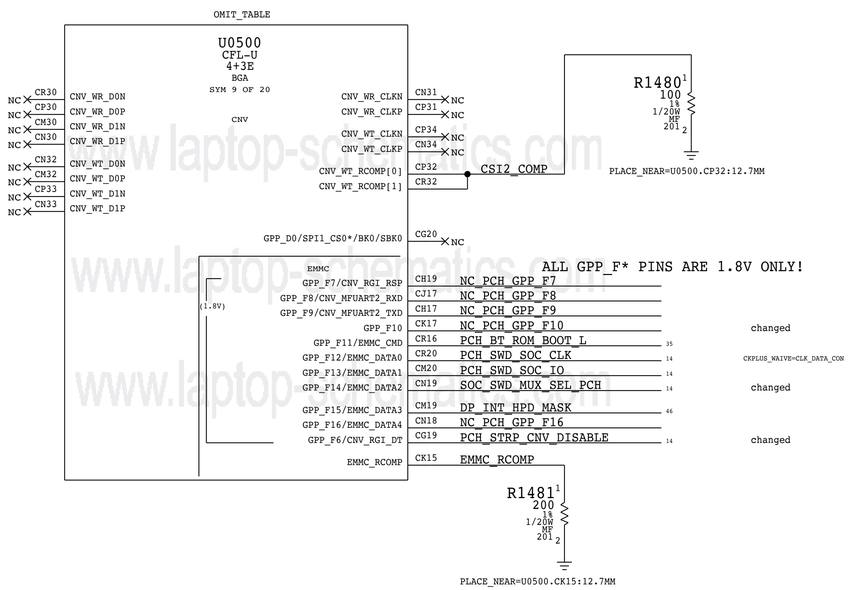

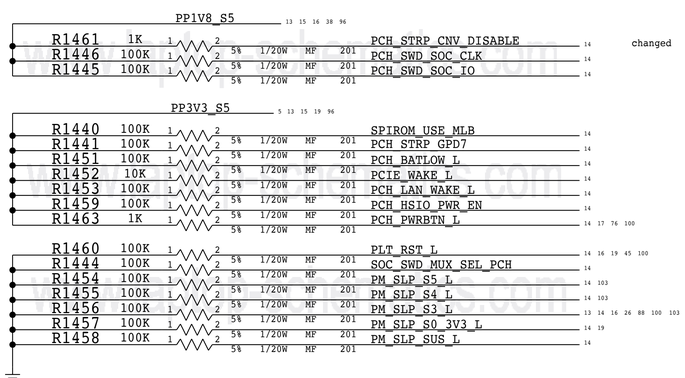

NOTE: =PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue Apr 5 13:08:54 2016

PAGE TITLE
PCH Power Management

Apple Inc.

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PCIe Port Assignments:

OMIT_TABLE

U0500
CFL-U
4+3E
BGA
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Port	Signal	Pin	Net
EXT A (SS,DCI)	USB3_EXTA_D2R_N	CB5	PCIE1_RXN/USB31_1_RXN
	USB3_EXTA_D2R_P	CB6	PCIE1_RXP/USB31_1_RXP
	USB3_EXTA_R2D_C_N	CA4	PCIE1_TXN/USB31_1_TXN
	USB3_EXTA_R2D_C_P	CA3	PCIE1_TXP/USB31_1_TXP
Fixture USB-A	TP_USB3_EXTC_D2R_N	BY8	PCIE2_RXN/USB31_2_RXN
	TP_USB3_EXTC_D2R_P	BY9	PCIE2_RXP/USB31_2_RXP
	TP_USB3_EXTC_R2D_C_N	CA2	PCIE2_TXN/USB31_2_TXN
	TP_USB3_EXTC_R2D_C_P	CA1	PCIE2_TXP/USB31_2_TXP
AirPort	PCH_PCIE_WLAN_D2R_N	BY7	PCIE3_RXN/USB31_3_RXN
	PCH_PCIE_WLAN_D2R_P	BY6	PCIE3_RXP/USB31_3_RXP
	PCH_PCIE_WLAN_R2D_C_N	BY4	PCIE3_TXN/USB31_3_TXN
	PCH_PCIE_WLAN_R2D_C_P	BY3	PCIE3_TXP/USB31_3_TXP
EXT USB-A	USB3_EXTD_D2R_N	BW6	PCIE4_RXN/USB31_4_RXN
	USB3_EXTD_D2R_P	BW5	PCIE4_RXP/USB31_4_RXP
	USB3_EXTD_R2D_C_N	BW2	PCIE4_TXN/USB31_4_TXN
	USB3_EXTD_R2D_C_P	BW1	PCIE4_TXP/USB31_4_TXP
Thunderbolt X lane 0	PCIE_TBT_X_D2R_N<0>	BW9	PCIE5_RXN/USB31_5_RXN
	PCIE_TBT_X_D2R_P<0>	BW8	PCIE5_RXP/USB31_5_RXP
	PCIE_TBT_X_R2D_C_N<0>	BW4	PCIE5_TXN/USB31_5_TXN
	PCIE_TBT_X_R2D_C_P<0>	BW3	PCIE5_TXP/USB31_5_TXP
Thunderbolt X lane 1	PCIE_TBT_X_D2R_N<1>	BU6	PCIE6_RXN/USB31_6_RXN
	PCIE_TBT_X_D2R_P<1>	BU5	PCIE6_RXP/USB31_6_RXP
	PCIE_TBT_X_R2D_C_N<1>	BU4	PCIE6_TXN/USB31_6_TXN
	PCIE_TBT_X_R2D_C_P<1>	BU3	PCIE6_TXP/USB31_6_TXP
Thunderbolt X lane 2	PCIE_TBT_X_D2R_N<2>	BT7	PCIE7_RXN
	PCIE_TBT_X_D2R_P<2>	BT6	PCIE7_RXP
	PCIE_TBT_X_R2D_C_N<2>	BU2	PCIE7_TXN
	PCIE_TBT_X_R2D_C_P<2>	BU1	PCIE7_TXP
Thunderbolt X lane 3	PCIE_TBT_X_D2R_N<3>	BU9	PCIE8_RXN
	PCIE_TBT_X_D2R_P<3>	BU8	PCIE8_RXP
	PCIE_TBT_X_R2D_C_N<3>	BT4	PCIE8_TXN
	PCIE_TBT_X_R2D_C_P<3>	BT3	PCIE8_TXP
Thunderbolt T lane 0	PCIE_TBT_T_D2R_N<0>	BP5	PCIE9_RXN
	PCIE_TBT_T_D2R_P<0>	BP6	PCIE9_RXP
	PCIE_TBT_T_R2D_C_N<0>	BR2	PCIE9_TXN
	PCIE_TBT_T_R2D_C_P<0>	BR1	PCIE9_TXP
Thunderbolt T lane 1 ETHERNET (DEV ONLY)	PCIE_TBT_T_D2R_N<1>	BN6	PCIE10_RXN
	PCIE_TBT_T_D2R_P<1>	BN5	PCIE10_RXP
	PCIE_TBT_T_R2D_C_N<1>	BR4	PCIE10_TXN
	PCIE_TBT_T_R2D_C_P<1>	BR3	PCIE10_TXP
	PCH_PCIE_RCOMP_N	CE6	PCIE_RCOMP_N
	PCH_PCIE_RCOMP_P	CE5	PCIE_RCOMP_P
	XDP_CPU_PRDY_L	W1	PROC_PRDY*
	XDP_CPU_PREQ_L	W2	PROC_PREQ*
	NC_PCH_GPP_A7	CC32	GPP_A7/PIRQA*
Thunderbolt X lane 2	PCIE_TBT_T_D2R_N<2>	BN10	PCIE11_RXN/SATA0_RXN
	PCIE_TBT_T_D2R_P<2>	BN8	PCIE11_RXP/SATA0_RXP
	PCIE_TBT_T_R2D_C_N<2>	BN4	PCIE11_TXN/SATA0_TXN
	PCIE_TBT_T_R2D_C_P<2>	BN3	PCIE11_TXP/SATA0_TXP
Thunderbolt X lane 3	PCIE_TBT_T_D2R_N<3>	BL6	PCIE12_RXN/SATA1A_RXN
	PCIE_TBT_T_D2R_P<3>	BL5	PCIE12_RXP/SATA1A_RXP
	PCIE_TBT_T_R2D_C_N<3>	BN2	PCIE12_TXN/SATA1A_TXN
	PCIE_TBT_T_R2D_C_P<3>	BN1	PCIE12_TXP/SATA1A_TXP

Net	Pin	Signal	Port
PCIE13_RXN	BK6	PCIE_SOC_D2R_N<0>	SOC lane 0
PCIE13_RXP	BK5	PCIE_SOC_D2R_P<0>	
PCIE13_TXN	BM4	PCIE_SOC_R2D_C_N<0>	
PCIE13_TXP	BM3	PCIE_SOC_R2D_C_P<0>	
PCIE14_RXN	BJ6	PCIE_SOC_D2R_N<1>	SOC lane 1
PCIE14_RXP	BJ5	PCIE_SOC_D2R_P<1>	
PCIE14_TXN	BL2	PCIE_SOC_R2D_C_N<1>	
PCIE14_TXP	BL1	PCIE_SOC_R2D_C_P<1>	
PCIE15_RXN/SATA1B_RXN	BG5	PCIE_SOC_D2R_N<2>	SOC lane 2
PCIE15_RXP/SATA1B_RXP	BG6	PCIE_SOC_D2R_P<2>	
PCIE15_TXN/SATA1B_TXN	BL4	PCIE_SOC_R2D_C_N<2>	
PCIE15_TXP/SATA1B_TXP	BL3	PCIE_SOC_R2D_C_P<2>	
PCIE16_RXN/SATA2_RXN	BE5	PCIE_SOC_D2R_N<3>	SOC lane 3
PCIE16_RXP/SATA2_RXP	BE6	PCIE_SOC_D2R_P<3>	
PCIE16_TXN/SATA2_TXN	BJ4	PCIE_SOC_R2D_C_N<3>	
PCIE16_TXP/SATA2_TXP	BJ3	PCIE_SOC_R2D_C_P<3>	
USB2_1N	CE3	USB_EXTA_N	Not Used
USB2_1P	CE4	USB_EXTA_P	
USB2_2N	CE1	NC_USB_EXTBN	Not Used
USB2_2P	CE2	NC_USB_EXTBP	
USB2_3N	CG3	NC_USB_EXTCN	Not Used
USB2_3P	CG4	NC_USB_EXTCP	
USB2_4N	CD3	TP_USB_FIXT2_N	TP for Fixture
USB2_4P	CD4	TP_USB_FIXT2_P	
USB2_5N	CG5	NC_USB_EXTDN	Not Used
USB2_5P	CG6	NC_USB_EXTDP	
USB2_6N	CC1	USB2_UPC_XA_N	XA RP Debug Mux
USB2_6P	CC2	USB2_UPC_XA_P	
USB2_7N	CG8	USB2_UPC_TA_N	TA RP
USB2_7P	CG9	USB2_UPC_TA_P	
USB2_8N	CB8	USB2_UPC_XB_N	XB RP
USB2_8P	CB9	USB2_UPC_XB_P	
USB2_9N	CH5	USB2_UPC_TB_N	TB RP
USB2_9P	CH6	USB2_UPC_TB_P	
USB2_10N	CC3	TP_USB_FIXT1_N	TP for Fixture
USB2_10P	CC4	TP_USB_FIXT1_P	
USB2_COMP	CC5	PCH_USB2_COMP	
USB2_ID	CE8		
USB2_VBUSSENSE	CC6	PCH_USB2_VBUSSENSE	
GPP_E3/CPU_GP0	CE9	XDP_PCH_OBSFN_C1	
GPP_E4/DEVSLP0	CP8	XDP_PCH_OBSDATA_A0	
GPP_E5/DEVSLP1	CR8	XDP_PCH_OBSDATA_A1	
GPP_E6/DEVSLP2	CM8	XDP_PCH_OBSDATA_A2	
GPP_D22/SPI1_IO3	CH23	NC_SDCONN_OC_L	
GPP_D23/I2S_MCLK	CK23	NC_PCH_ENET_LOW_PWR	
GPP_D18/DMIC_DATA1	CJ25	NC_PCH_GPP_D18	
GPP_D19/DMIC_CLK0	CP24	NC_PCH_GPP_D19	
GPP_D20/DMIC_DATA0	CN24	NC_PCH_GPP_D20	
GPP_E0/SATAXPCIE0/SATAGP0	CN8	XDP_PCH_OBSDATA_D1	
GPP_E1/SATAXPCIE1/SATAGP1	CM10	XDP_PCH_OBSDATA_D2	
GPP_E2/SATAXPCIE2/SATAGP2	CP10	XDP_PCH_OBSDATA_D3	

PCIE/USB3/SATA

USB2

PLACE_NEAR=U0500.CE6:12.7mm

R1504 100 1% 1/20W MF 201

GROUNDED PER CFL EDS.

R1503 1K 5% 1/20W MF 201

PLACE_NEAR=U0500.CC6:12.7MM

R1501 113 1% 1/20W MF 201

PLACE_NEAR=U0500.CC5:12.7MM

OMIT_TABLE

U0500
CFL-U
4+3E
BGA
SYM 10 OF 20
CLOCK SIGNALS

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

Net	Pin	Signal
PCIE_CLK100M_TBT_T_N	AW2	CLKOUT_PCIE_N0
PCIE_CLK100M_TBT_T_P	AY3	CLKOUT_PCIE_P0
TBT_T_CLKREQ_L	CF32	GPP_B5/SRCCLKREQ0*
PCIE_CLK100M_SOC_N	BC1	CLKOUT_PCIE_N1
PCIE_CLK100M_SOC_P	BC2	CLKOUT_PCIE_P1
SOC_CLKREQ_L	CE32	GPP_B6/SRCCLKREQ1*
PCIE_CLK100M_TBT_X_N	BD3	CLKOUT_PCIE_N2
PCIE_CLK100M_TBT_X_P	BC3	CLKOUT_PCIE_P2
TBT_X_CLKREQ_L	CF30	GPP_B7/SRCCLKREQ2*
NC_PCIE_CLK100M4N	BH3	CLKOUT_PCIE_N3
NC_PCIE_CLK100M4P	BH4	CLKOUT_PCIE_P3
NC_ENETSD_CLKREQ_L	CE31	GPP_B8/SRCCLKREQ3*
PCH_PCIE_CLK100M_WLAN_N	BA1	CLKOUT_PCIE_N4
PCH_PCIE_CLK100M_WLAN_P	BA2	CLKOUT_PCIE_P4
PCH_WLAN_CLKREQ_L	CE30	GPP_B9/SRCCLKREQ4*
NC_PCIE_CLK100M5N	BE1	CLKOUT_PCIE_N5
NC_PCIE_CLK100M5P	BE2	CLKOUT_PCIE_P5
NC_DEBUG_CLKREQ5_L	CF31	GPP_B10/SRCCLKREQ5*
CLKOUT_ITPXDP_N	AU1	NC_ITPXDP_CLK100MN
CLKOUT_ITPXDP_P	AU2	NC_ITPXDP_CLK100MP
GPD8/SUSCLK	BT32	NC_PCH_CLK32K_SUS
XTAL_IN	CK3	PCH_CLK24M_XTALIN
XTAL_OUT	CK2	PCH_CLK24M_XTALOUT
CLKIN_XTAL	CM3	PCH_CLKIN_XTAL
CLK_BIASREF	CJ1	PCH_DIFFCLK_BIASREF
RTCX1	BN31	PMU_CLK32K_PCH_1V0
RTCX2	BN32	NC
SRTCRST*	BR37	PCH_RTC_RESET_L
RTCRST*	BR34	PCH_RTC_RESET_L

R1573 100K 1% 1/20W MF 201

PMU_CLK32K_PCH

R1572 127K 1% 1/20W MF 201

PLACE_NEAR=U0500.BN31:5MM
PLACE_NEAR=U0500.BN31:5MM

PP1V8_S5

R1533 47K 5% 1/20W MF 201 — SOC_CLKREQ_L
R1534 47K 5% 1/20W MF 201 — PCH_WLAN_CLKREQ_L

PP3V3_S5

R1531 47K 5% 1/20W MF 201 — TBT_X_CLKREQ_L
R1532 47K 5% 1/20W MF 201 — TBT_T_CLKREQ_L

R1521 0 5% 1/20W MF 0201 — PCH_CLKIN_XTAL
PLACE_NEAR=U0500.CM3:25.4mm

R1520 60.4 1% 1/20W MF 201 — PCH_DIFFCLK_BIASREF
PLACE_NEAR=U0500.CJ1:25.4mm

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Thu Jun 18 20:05:18 2015

PAGE TITLE
PCH PCIE/USB/CLKS

Apple Inc.

DRAWING NUMBER 051-02166
SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
PAGE 15 OF 150
SHEET 15 OF 108

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ALL GPP_F* PINS ARE 1.8V ONLY!

OMIT_TABLE

100 45 19 14 IN PLT_RST_L

R1675 100K 5% 1/20W MF 201

38 OUT

U0500
CFL-U
4+3E
BGA
SYM 6 OF 20

LPSS		
GPP_B15/GSPI0_CS0*		
GPP_B16/GSPI0_CLK		
GPP_B17/GSPI0_MISO		
GPP_B18/GSPI0_MOSI		
	(STRAP)	
GPP_B19/GSPI1_CS0*		
GPP_B20/GSPI1_CLK		
GPP_B21/GSPI1_MISO		
GPP_B22/GSPI1_MOSI		
	(STRAP)	
GPP_C8/UART0_RXD		
GPP_C9/UART0_TXD		(1.8V)
GPP_C10/UART0_RTS*		(1.8V)
GPP_C11/UART0_CTS*		
GPP_C16/I2C0_SDA		
GPP_C17/I2C0_SCL		
GPP_C18/I2C1_SDA		
GPP_C19/I2C1_SCL		
GPP_C12/UART1_RXD/ISH_UART1_RXD		
GPP_C13/UART1_TXD/ISH_UART1_TXD		
GPP_C14/UART1_RTS*/ISH_UART1_RTS*		
GPP_C15/UART1_CTS*/ISH_UART1_CTS*		
GPP_E22/DPPD_CTRLCLK		
GPP_E23/DPPD_CTRLDATA		
GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK		(1.8V)
GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK		(1.8V)
GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI		(1.8V)
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO		(1.8V)
GPP_B3/CPU_GP2		
GPP_B4/CPU_GP3		

37 16	PCH_SOC_SYNC	CC27
	SOC_PERST_L	CE28
	NC_PCH_ENETSD_RESET_L	CE27
16	PCH_STRP_NO_REBOOT	CE29
	NC_PCH_GPP_B19	CA31
	NC_PCH_GPP_B20	CC29
	NC_PCH_GPP_B21	CC30
	NC_PCH_STRP_BOOT_SPI_L	CA30
34 16 IN	PCH_UART_BT_D2R	CR14
34 16 OUT	PCH_UART_BT_R2D	CP14
34 16 OUT	PCH_UART_BT_RTS_L	CN14
34 16 IN	PCH_UART_BT_CTS_L	CM14
	NC_PCH_GPP_C16	CM11
	NC_PCH_GPP_C17	CN11
	NC_PCH_GPP_C18	CK12
	NC_PCH_GPP_C19	CJ12
	NC_PCH_GPP_C12	CG12
	NC_PCH_GPP_C13	CH12
	NC_PCH_GPP_C14	CF12
	NC_PCH_GPP_C15	CG14
	NC_MEM_OK	CP4
	NC_PCH_DDPD_CTRLDATA	CN4
	NC_PCH_I2S_BT_CLK	CH32
	NC_PCH_I2S_BT_SYNC	CJ32
	NC_PCH_I2S_BT_R2D	CH29
	NC_PCH_I2S_BT_D2R	CH30
36 35 19 OUT	PCH_WLAN_PERST_L	CB34
36 35 OUT	PCH_WLAN_DEV_WAKE	CC35

ISH		
GPP_D5/ISH_I2C0_SDA	CK22	NC_PCH_GPP_D5
GPP_D6/ISH_I2C0_SCL	CH20	NC_PCH_GPP_D6
GPP_D7/ISH_I2C1_SDA	CH22	NC_PCH_GPP_D7
GPP_D8/ISH_I2C1_SCL	CJ22	NC_PCH_UPC_I2C_INT_L
GPP_D1/SPI1_CLK	CF20	NC_PCH_GPP_D1
GPP_D2/SPI1_MISO_IO1	CG22	NC_PCH_GPP_D2
GPP_D3/SPI1_MOSI_IO0	CF22	NC_PCH_GPP_D3
GPP_D4/IMGCLKOUT0	CG25	NC_PCH_GPP_D4
GPP_F4/CNV_BRI_DT	CJ20	NC_PCH_GPP_F4
GPP_F5/CNV_BRI_RSP	CK20	NC_PCH_GPP_F5
GPP_G6/SD_CLK	CK36	TBT_X_DPMUX_SEL (IN 28)
GPP_D9	CN22	TBT_X_PLUG_EVENT_L
GPP_D10	CR22	TBT_T_PLUG_EVENT_L
GPP_G7/SD_WP	CK34	TBT_T_DPMUX_SEL (IN 28)
GPP_G2/SD3_DATA1	CL36	TBT_T_CIO_PWR_EN (OUT 16 88 90 91 92)
GPP_G3/SD3_DATA2	CM35	TBT_T_USB_PWR_EN (OUT 16 88 90 91 92)
GPP_G4/SD_DATA3	CN35	TBT_X_PCI_RESET_L (OUT 19 26 28)
GPP_G5/SD_CD*	CH35	TBT_T_PCI_RESET_L (OUT 19 88 90)
GPP_A18/ISH_GP0	BW35	NC_PCH_GPP_A18
GPP_A19/ISH_GP1	BW34	NC_PCH_GPP_A19
GPP_A20/ISH_GP2	CA37	NC_PCH_GPP_A20
GPP_A21/ISH_GP3	CA36	NC_PCH_GPP_A21
GPP_A22/ISH_GP4	CA35	NC_BTI2SMUX_SEL_PCH
GPP_A23/ISH_GP5	CA34	NC_PCH_BT_DEV_WAKE
GPP_A12/ISH_GP6/BM_BUSY*/SX_EXIT_HOLDOFF*	BW37	NC_PCH_GPP_A12

PM_SLP_S3_L 13 14 16 26 88 100 103

R1670 100K 5% 1/20W MF 201

R1671 100K 5% 1/20W MF 201

IN 26 28

IN 88 90

PP1V8_S5 13 14 15 38 96

R1662	47K	5%	1/20W	MF	201		PCH_UART_BT_D2R (16 34)
R1663	47K	5%	1/20W	MF	201		PCH_UART_BT_R2D (16 34)
R1664	47K	5%	1/20W	MF	201		PCH_UART_BT_RTS_L (16 34)
R1665	47K	5%	1/20W	MF	201		PCH_UART_BT_CTS_L (16 34)
R1656	1K	5%	1/20W	MF	201		PCH_STRP_NO_REBOOT (16)

PP3V3_TBT_T_S0 97

R1676	100K	5%	1/20W	MF	201		TBT_T_CIO_PWR_EN (16 88 90 91 92)
R1677	100K	5%	1/20W	MF	201	NOSTUFF	TBT_T_USB_PWR_EN (16 88 90 91 92)

PM_SLP_S3_L 13 14 16 26 88 100 103

R1678	100K	5%	1/20W	MF	201		TBT_T_CIO_PWR_EN (16 88 90 91 92)
R1679	100K	5%	1/20W	MF	201		TBT_T_USB_PWR_EN (16 88 90 91 92)
R1674	100K	5%	1/20W	MF	201		PCH_SOC_SYNC (16 37)

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Wed Oct 28 12:50:22 2015

PAGE TITLE
PCH SPI/UART/GPIO

Apple Inc.

DRAWING NUMBER 051-02166
SIZE D
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BRANCH evt-mars-0
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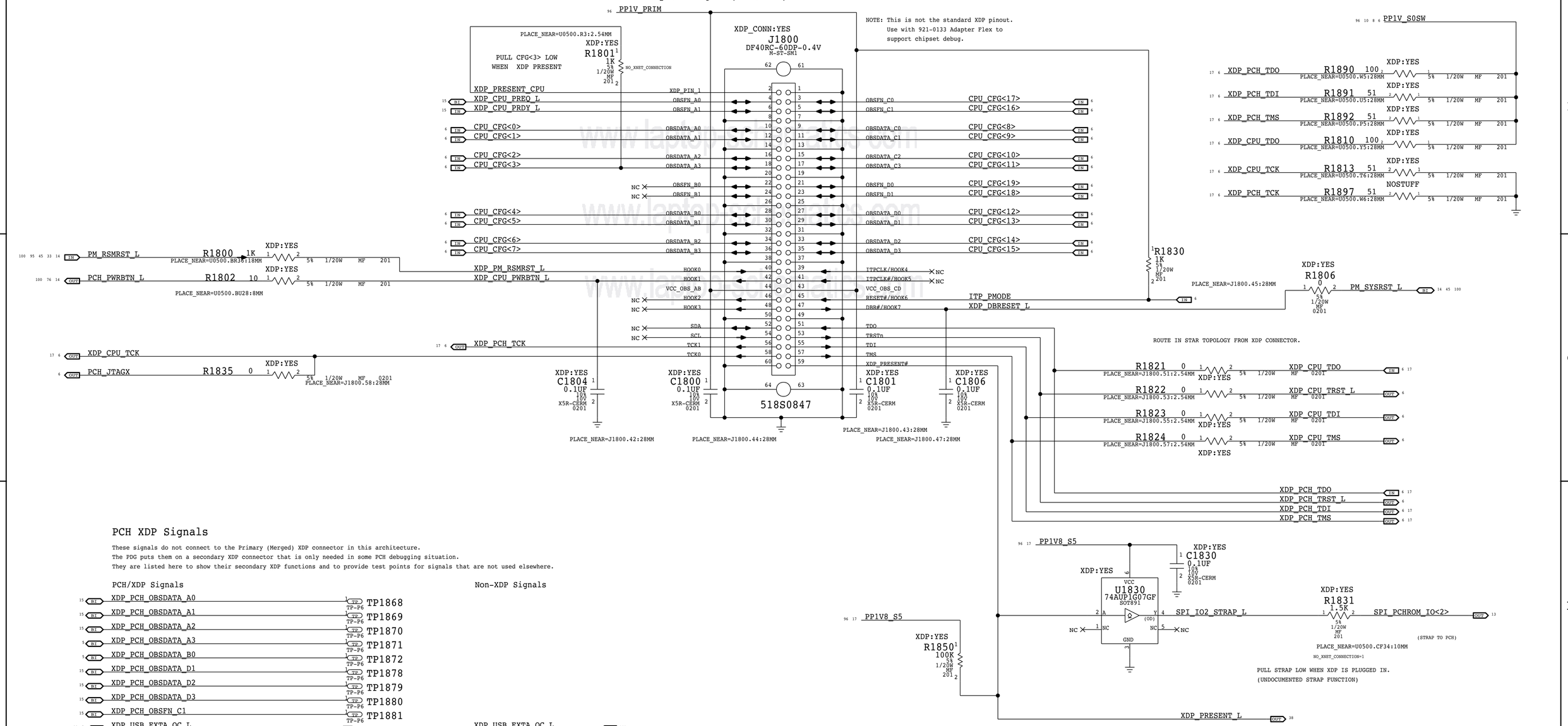
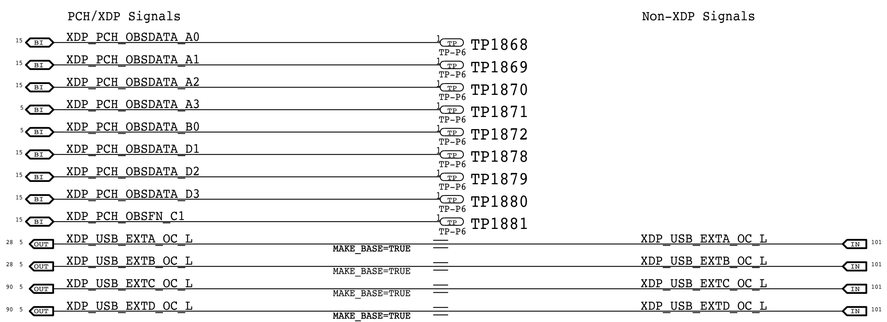
Primary / Merged (CPU/PCH) Micro2-XDP



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.



Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

PAGE TITLE	CPU/PCH Merged XDP
Apple Inc.	DRAWING NUMBER 051-02166 SIZE D
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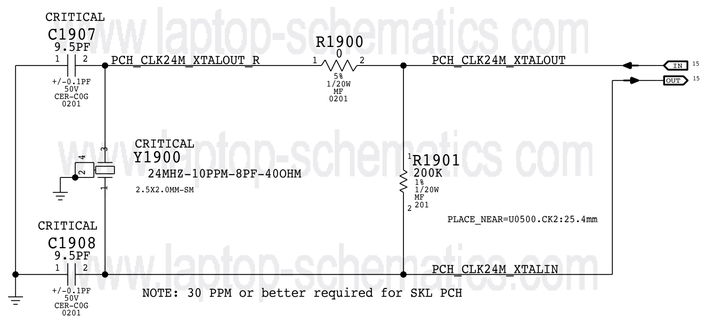
24MHz CLOCK



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J132_JIN SYNC_DATE=06/05/2017

PAGE TITLE
Chipset Support 1

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DRAWING NUMBER 051-02166 SIZE D

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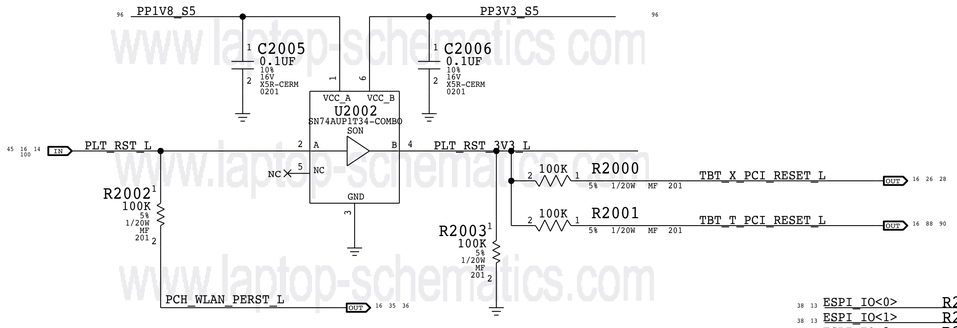
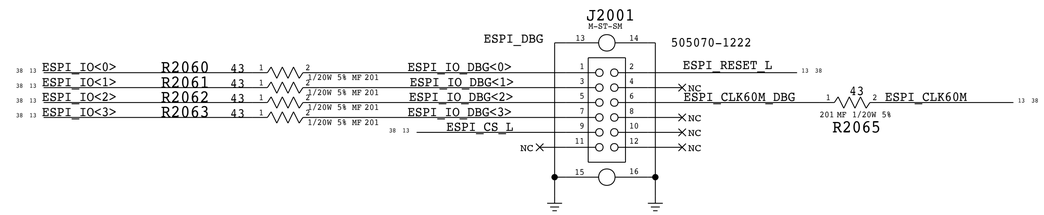
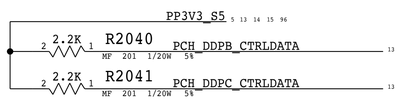
Platform Reset Connections



eSPI Analyzer
Placement study first



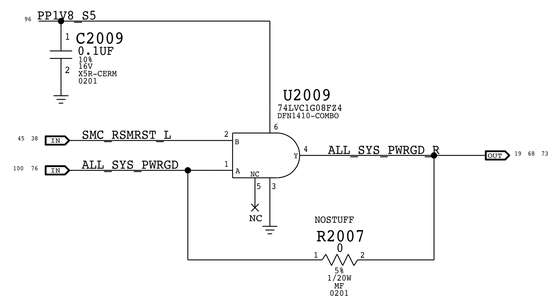
ENABLE DDPB DDPC INTERFACES



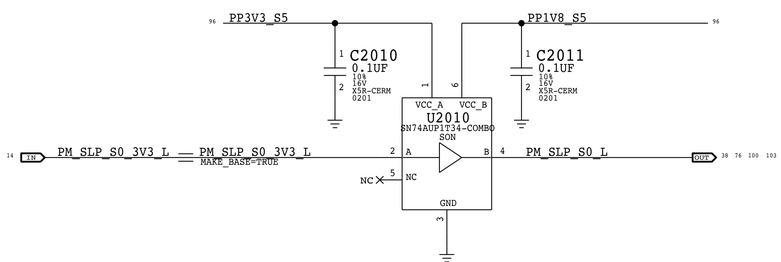
SIGNAL ALIASES

PCH_RTC_RESET_L	MAKE_BASE=TRUE PCH_RTC_RESET_L MAKE_BASE=TRUE	
TEST_NOA_N_10	MAKE_BASE=TRUE TEST_NOA_N_10 MAKE_BASE=TRUE	
TEST_NOA_N_11	TEST_NOA_N_11 MAKE_BASE=TRUE	NO_TEST=1
XDP_BPM_L<3..1>	NC_XDP_BPM_L<3..1>	

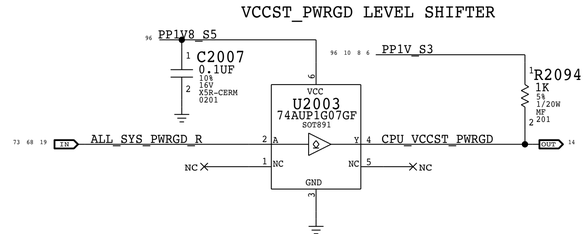
ALL_SYS_PWRGD QUALIFIER



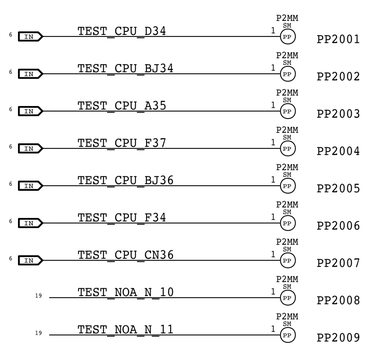
SLP_S0# LEVEL SHIFTER



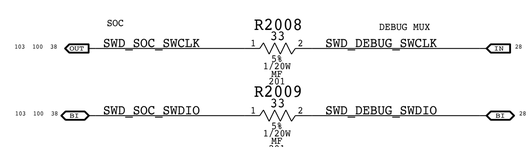
VCCST_PWRGD LEVEL SHIFTER



TPs for Chipset Debug Pins



SOC SWD <=> DEBUG MUX PATH



BOM_COST_GROUP=CPU & CHIPSET 15:06:19

SYNC_MASTER=J132_J18 SYNC_DATE=09/05/2017

PAGE TITLE
Chipset Support 2

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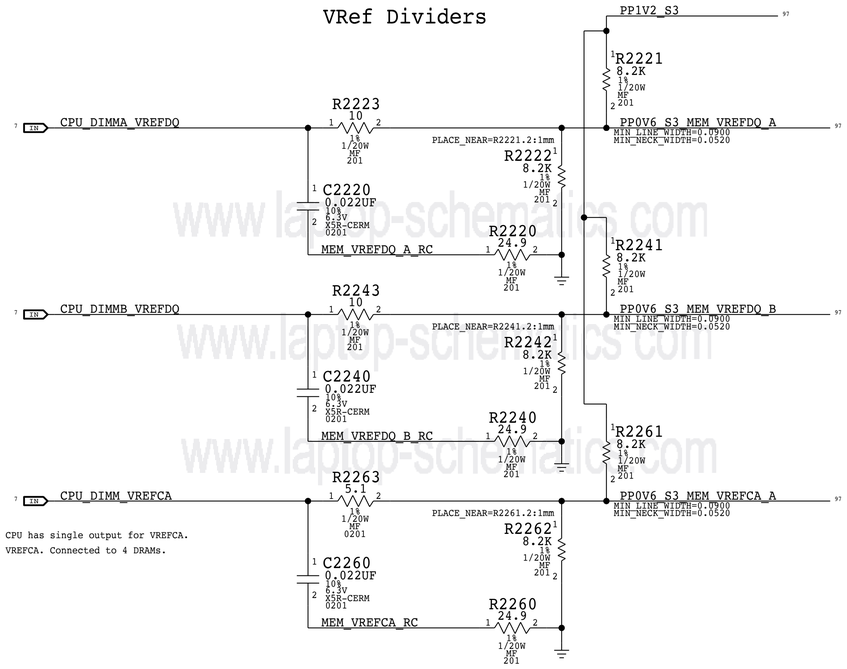
CPU-Based Margining

VRef Dividers



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

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BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

PAGE TITLE
LPDDR3 VREF Margining

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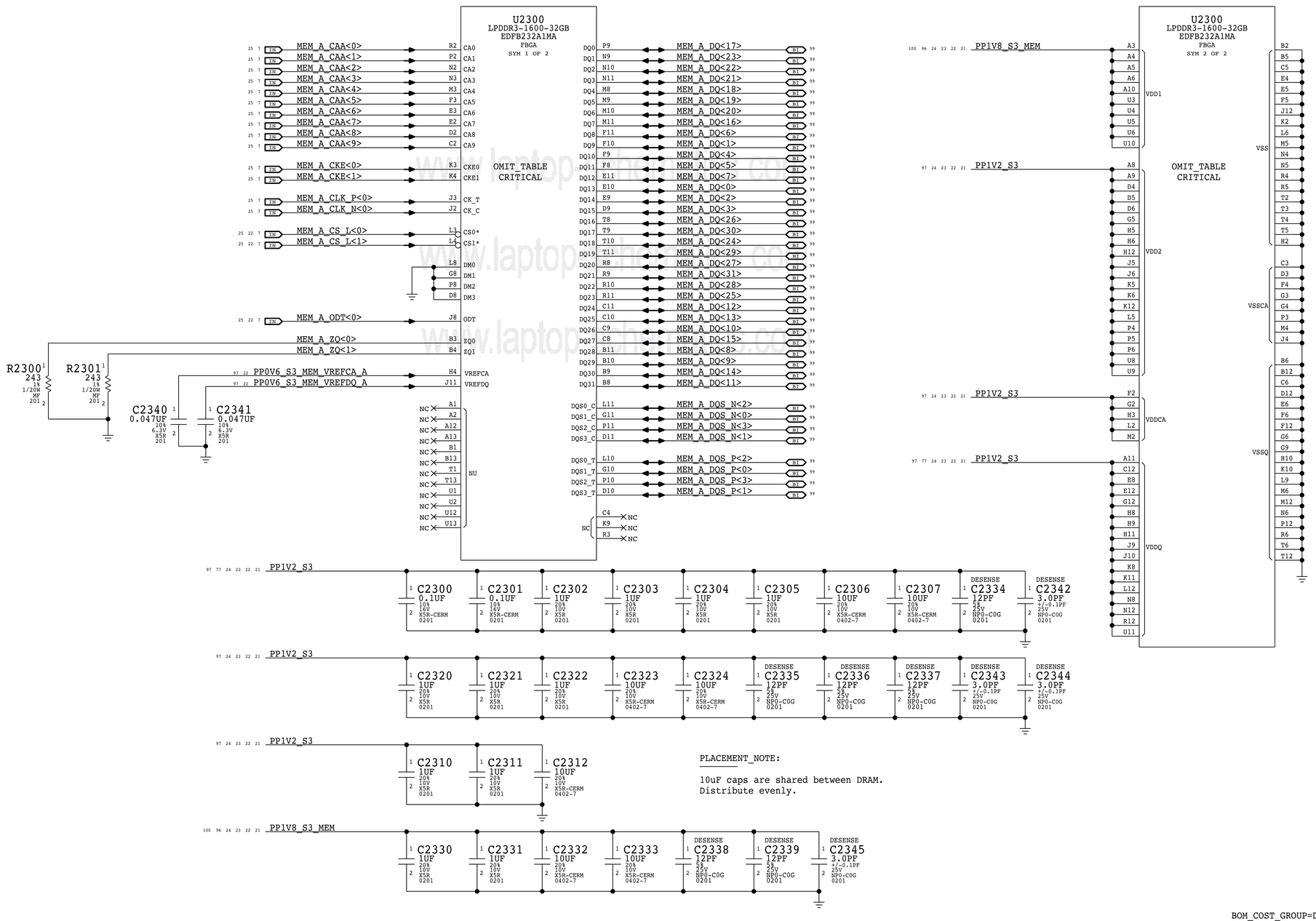
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

PAGE TITLE
LPDDR3 DRAM Channel A (00-31)

Apple Inc.

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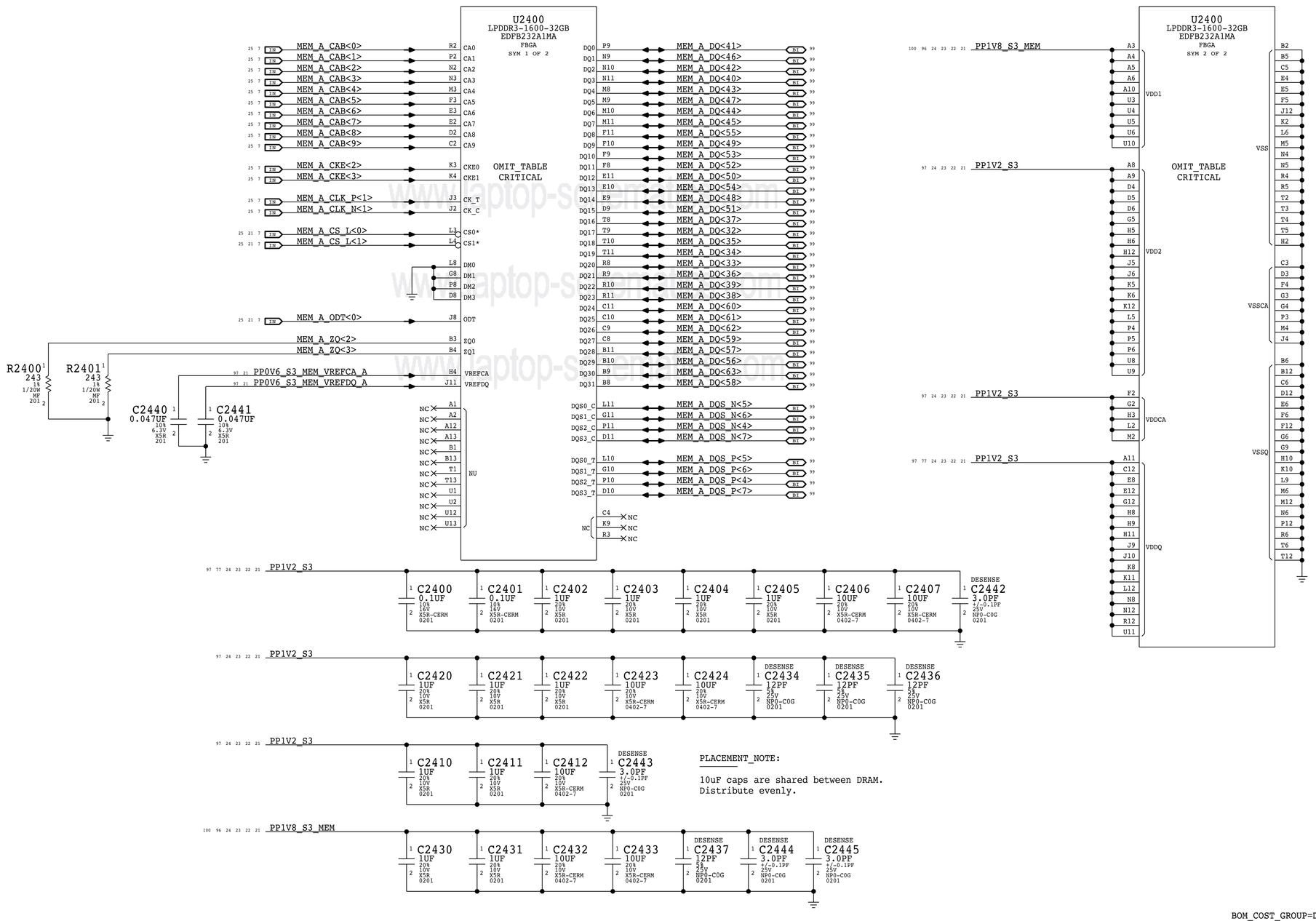
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

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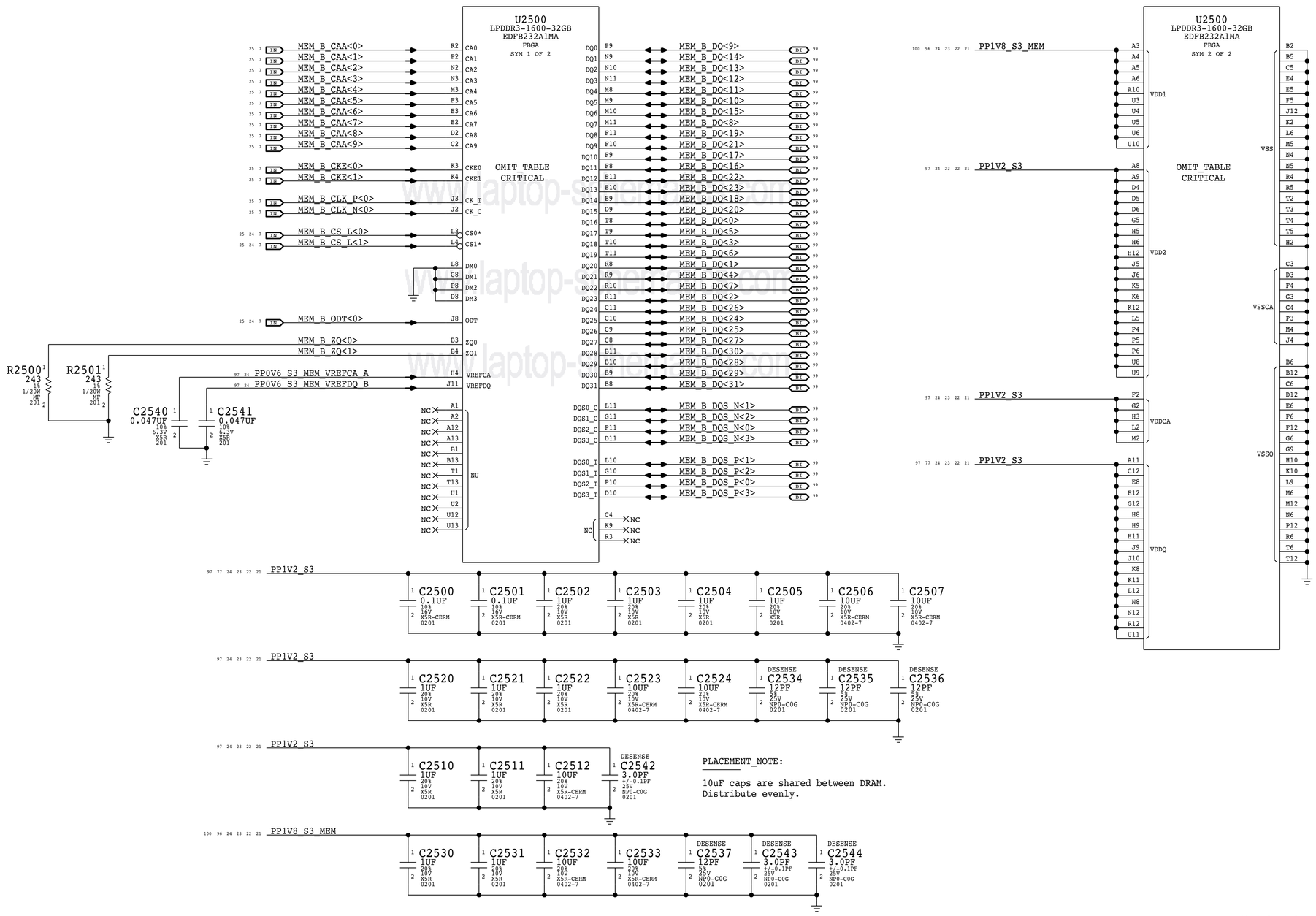
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

PAGE TITLE
LPDDR3 DRAM Channel B (00-31)

Apple Inc.

DRAWING NUMBER	051-02166
SIZE	D
REVISION	4.0.0
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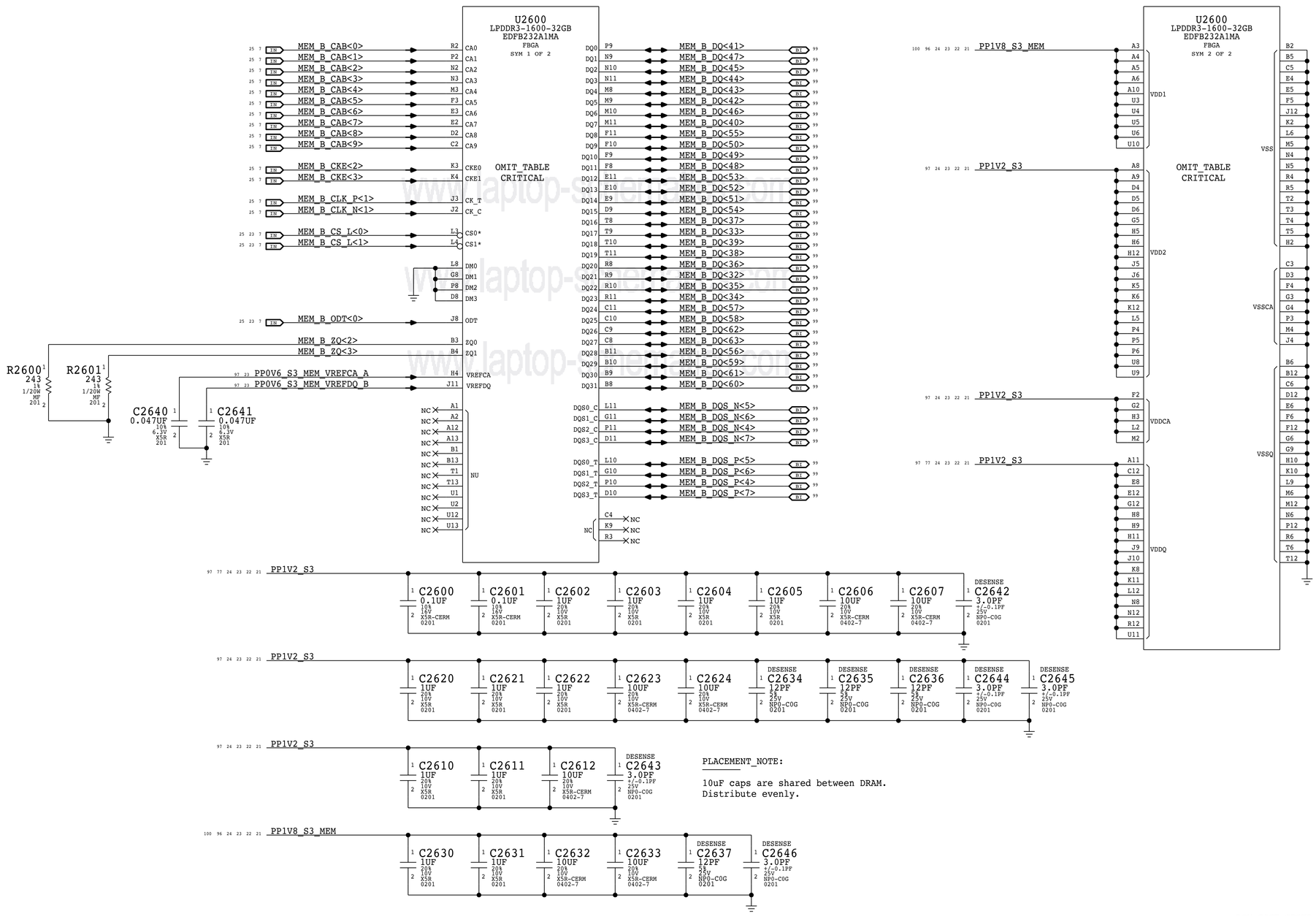
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER	051-02166
SIZE	D
REVISION	4.0.0
BRANCH	evt-mars-0
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Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

97 PP0V6_S0_DDRVTT

21 7	IN	MEM_A_CAA<9>	R2700	68	1%	1/20W	201	MF	C2700 0.47UF 20% 4V CERM-X5R-1 201	DESENSE C2730 12PF 5% 25V NPO-COG 0201
21 7	IN	MEM_A_CAA<8>	R2701	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<6>	R2702	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<7>	R2703	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<5>	R2704	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CLK_P<0>	R2705	39	1%	1/20W	201	MF	C2701 0.47UF 20% 4V CERM-X5R-1 201	C2702 0.47UF 20% 4V CERM-X5R-1 201
21 7	IN	MEM_A_CLK_N<0>	R2706	39	1%	1/20W	201	MF		
21 7	IN	MEM_A_CKE<1>	R2707	82	1%	1/20W	201	MF		
21 7	IN	MEM_A_CKE<0>	R2708	82	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<4>	R2709	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<3>	R2710	68	1%	1/20W	201	MF	C2703 0.47UF 20% 4V CERM-X5R-1 201	C2704 0.47UF 20% 4V CERM-X5R-1 201
21 7	IN	MEM_A_CAA<2>	R2711	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<1>	R2712	68	1%	1/20W	201	MF		
21 7	IN	MEM_A_CAA<0>	R2713	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<9>	R2714	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<8>	R2715	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<6>	R2716	68	1%	1/20W	201	MF	C2705 0.47UF 20% 4V CERM-X5R-1 201	C2706 0.47UF 20% 4V CERM-X5R-1 201
22 7	IN	MEM_A_CAB<7>	R2717	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<5>	R2718	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CLK_P<1>	R2719	39	1%	1/20W	201	MF		
22 7	IN	MEM_A_CLK_N<1>	R2720	39	1%	1/20W	201	MF		
22 7	IN	MEM_A_CKE<2>	R2721	82	1%	1/20W	201	MF		
22 7	IN	MEM_A_CKE<3>	R2722	82	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<4>	R2723	68	1%	1/20W	201	MF	C2707 0.47UF 20% 4V CERM-X5R-1 201	C2708 0.47UF 20% 4V CERM-X5R-1 201
22 7	IN	MEM_A_CAB<2>	R2724	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<3>	R2725	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<1>	R2726	68	1%	1/20W	201	MF		
22 7	IN	MEM_A_CAB<0>	R2727	68	1%	1/20W	201	MF		
22 21 7	IN	MEM_A_CS_L<0>	R2728	82	1%	1/20W	201	MF		
22 21 7	IN	MEM_A_CS_L<1>	R2729	82	1%	1/20W	201	MF	C2709 0.47UF 20% 4V CERM-X5R-1 201	
22 21 7	IN	MEM_A_ODT<0>	R2730	82	1%	1/20W	201	MF		
									CRITICAL C2720 20UF 20% 6.3V CERM-X5R 0402	DESENSE C2722 3.0PF ±0.1PF 25V NPO-COG 0201

97 PP0V6_S0_DDRVTT

23 7	IN	MEM_B_CAA<9>	R2740	68	1%	1/20W	201	MF	C2710 0.47UF 20% 4V CERM-X5R-1 201	DESENSE C2731 12PF 5% 25V NPO-COG 0201
23 7	IN	MEM_B_CAA<8>	R2741	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<7>	R2742	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<6>	R2743	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<5>	R2744	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CLK_P<0>	R2745	39	1%	1/20W	201	MF	C2711 0.47UF 20% 4V CERM-X5R-1 201	C2712 0.47UF 20% 4V CERM-X5R-1 201
23 7	IN	MEM_B_CLK_N<0>	R2746	39	1%	1/20W	201	MF		
23 7	IN	MEM_B_CKE<1>	R2747	82	1%	1/20W	201	MF		
23 7	IN	MEM_B_CKE<0>	R2748	82	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<4>	R2749	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<2>	R2750	68	1%	1/20W	201	MF	C2713 0.47UF 20% 4V CERM-X5R-1 201	C2714 0.47UF 20% 4V CERM-X5R-1 201
23 7	IN	MEM_B_CAA<3>	R2751	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<1>	R2752	68	1%	1/20W	201	MF		
23 7	IN	MEM_B_CAA<0>	R2753	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<9>	R2754	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<8>	R2755	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<7>	R2756	68	1%	1/20W	201	MF	C2715 0.47UF 20% 4V CERM-X5R-1 201	C2716 0.47UF 20% 4V CERM-X5R-1 201
24 7	IN	MEM_B_CAB<6>	R2757	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<5>	R2758	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CLK_N<1>	R2759	39	1%	1/20W	201	MF		
24 7	IN	MEM_B_CLK_P<1>	R2760	39	1%	1/20W	201	MF		
24 7	IN	MEM_B_CKE<2>	R2761	82	1%	1/20W	201	MF		
24 7	IN	MEM_B_CKE<3>	R2762	82	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<4>	R2763	68	1%	1/20W	201	MF	C2717 0.47UF 20% 4V CERM-X5R-1 201	C2718 0.47UF 20% 4V CERM-X5R-1 201
24 7	IN	MEM_B_CAB<2>	R2764	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<3>	R2765	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<1>	R2766	68	1%	1/20W	201	MF		
24 7	IN	MEM_B_CAB<0>	R2767	68	1%	1/20W	201	MF		
24 23 7	IN	MEM_B_CS_L<0>	R2768	82	1%	1/20W	201	MF		
24 23 7	IN	MEM_B_CS_L<1>	R2769	82	1%	1/20W	201	MF	C2719 0.47UF 20% 4V CERM-X5R-1 201	
24 23 7	IN	MEM_B_ODT<0>	R2770	82	1%	1/20W	201	MF		
									CRITICAL C2740 20UF 20% 6.3V CERM-X5R 0402	DESENSE C2742 3.0PF ±0.1PF 25V NPO-COG 0201

BOM_COST_GROUP=DRAM

SYNC_MASTER=J79A_MLB SYNC_DATE=01/31/2017

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D

REVISION 4.0.0

BRANCH evt-mars-0

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SHEET 25 OF 108

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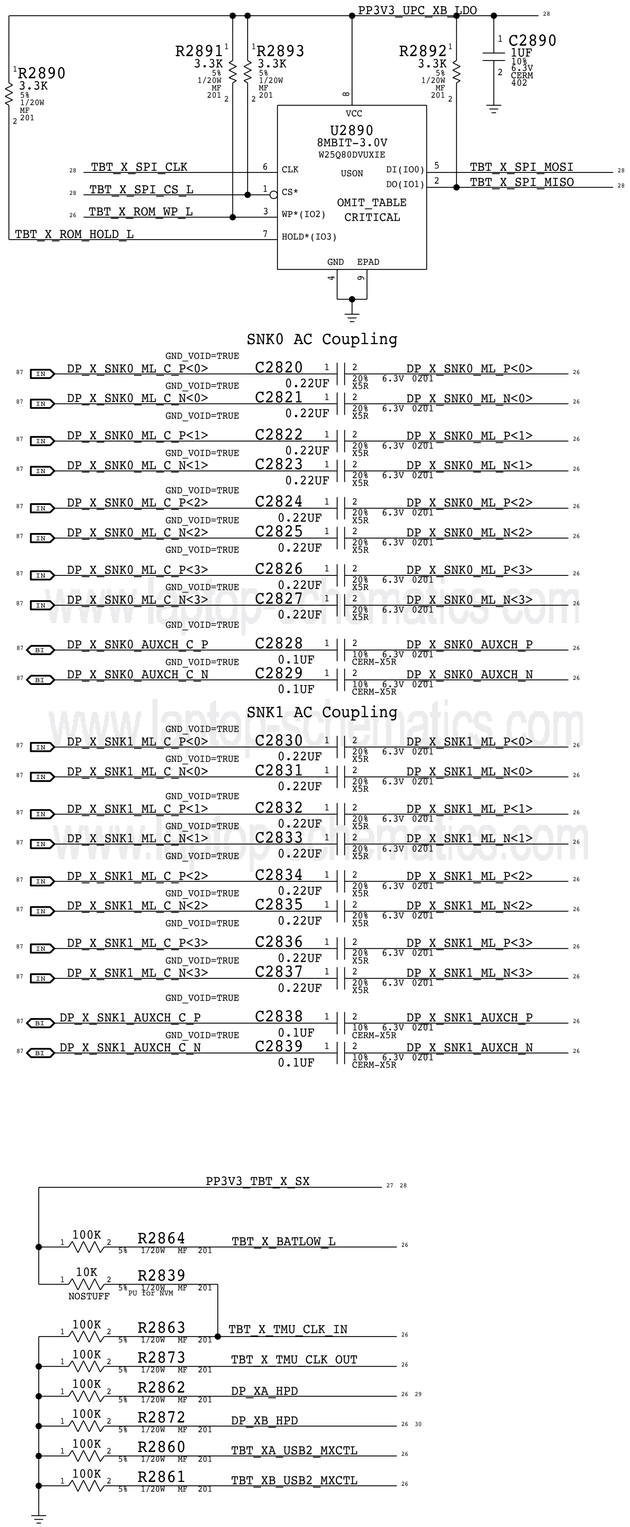

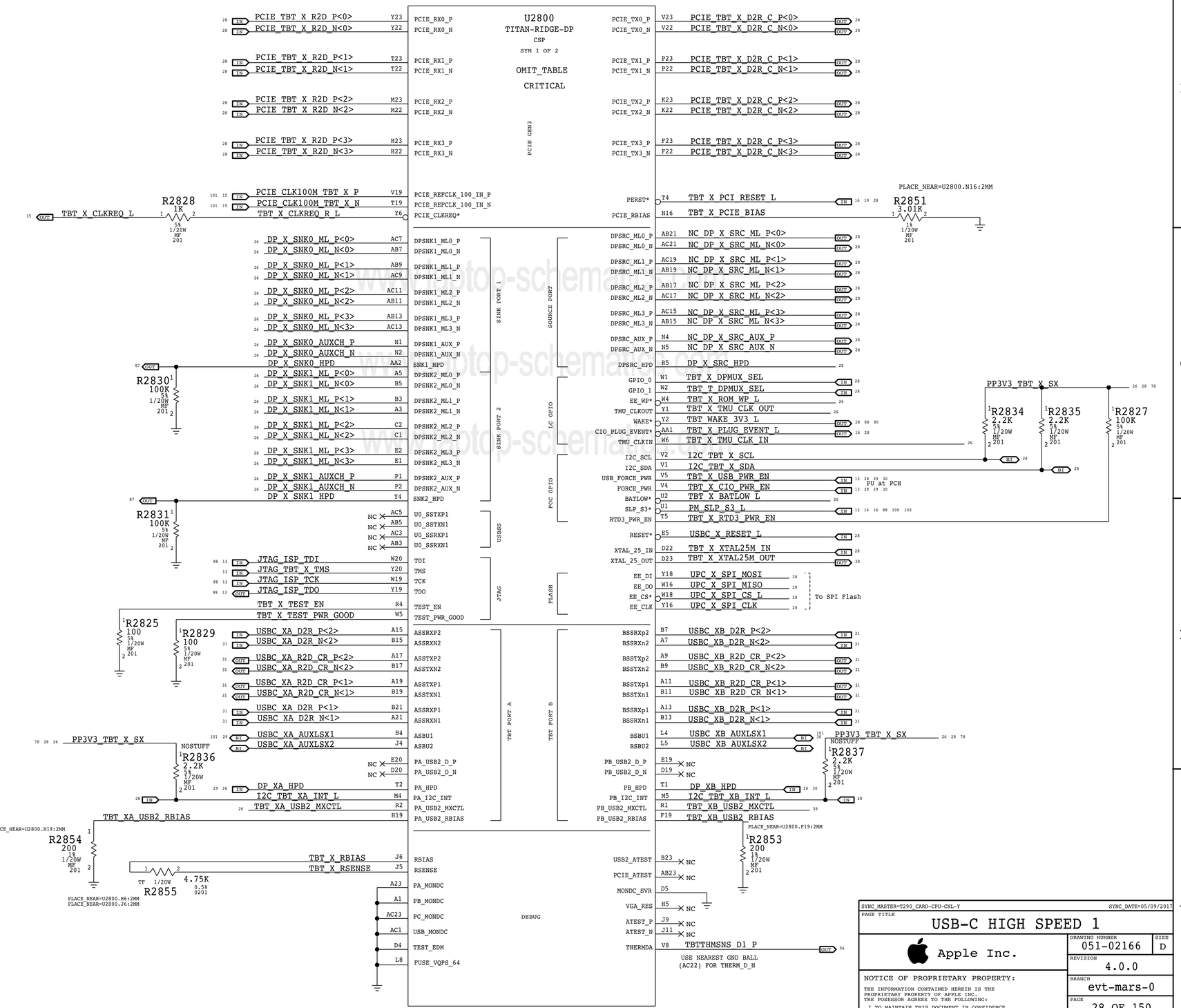

SYNC_MASTER=T290_CARD-CPU-CNL-Y SYNC_DATE=05/09/2017

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USB-C HIGH SPEED 1

Apple Inc.

DRAWING NUMBER	051-02166
SIZE	D
REVISION	4.0.0
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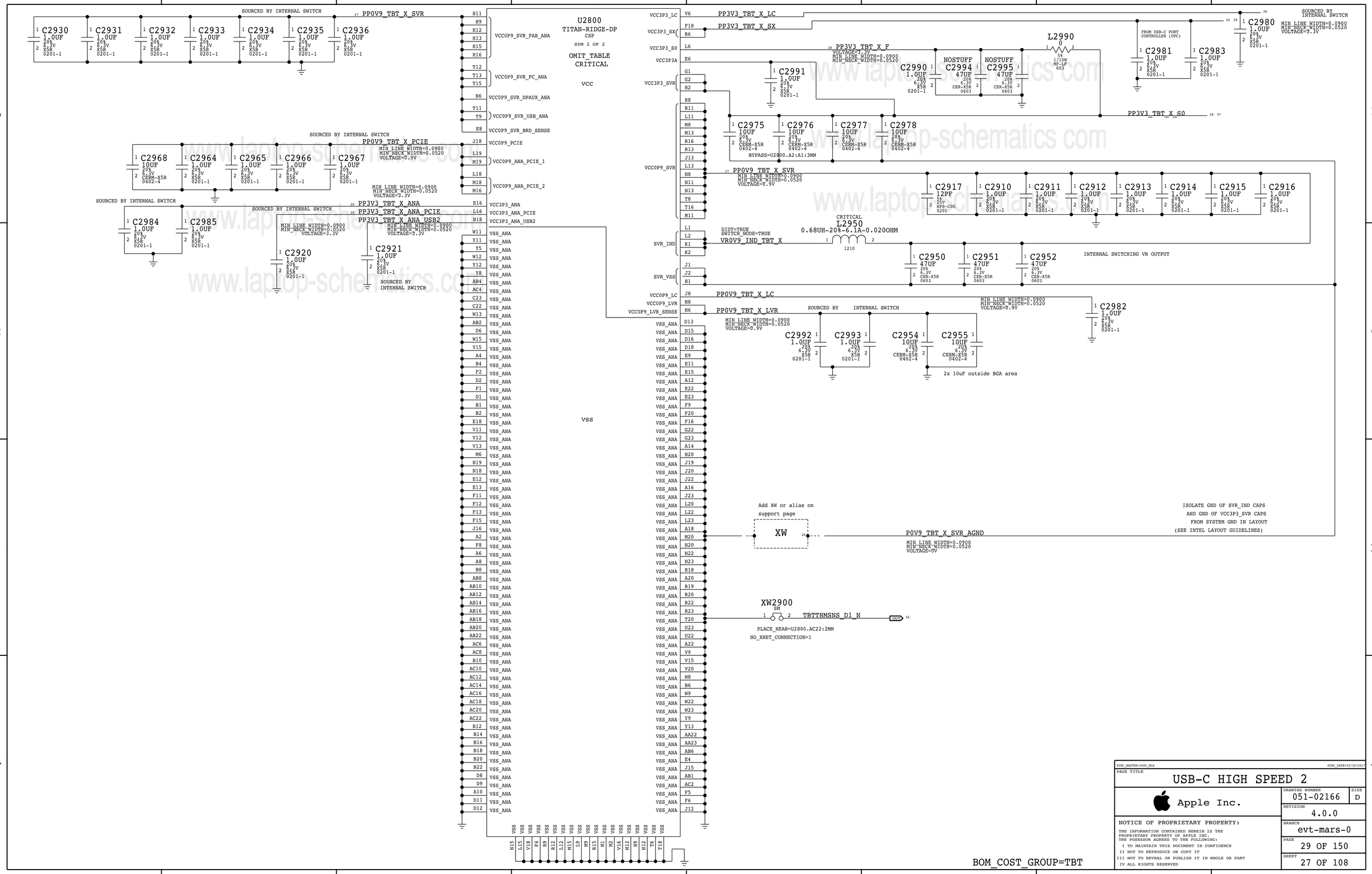

SYNC_MASTER=J680_MLB SYNC_DATE=03/30/2017

PAGE TITLE

USB-C HIGH SPEED 2

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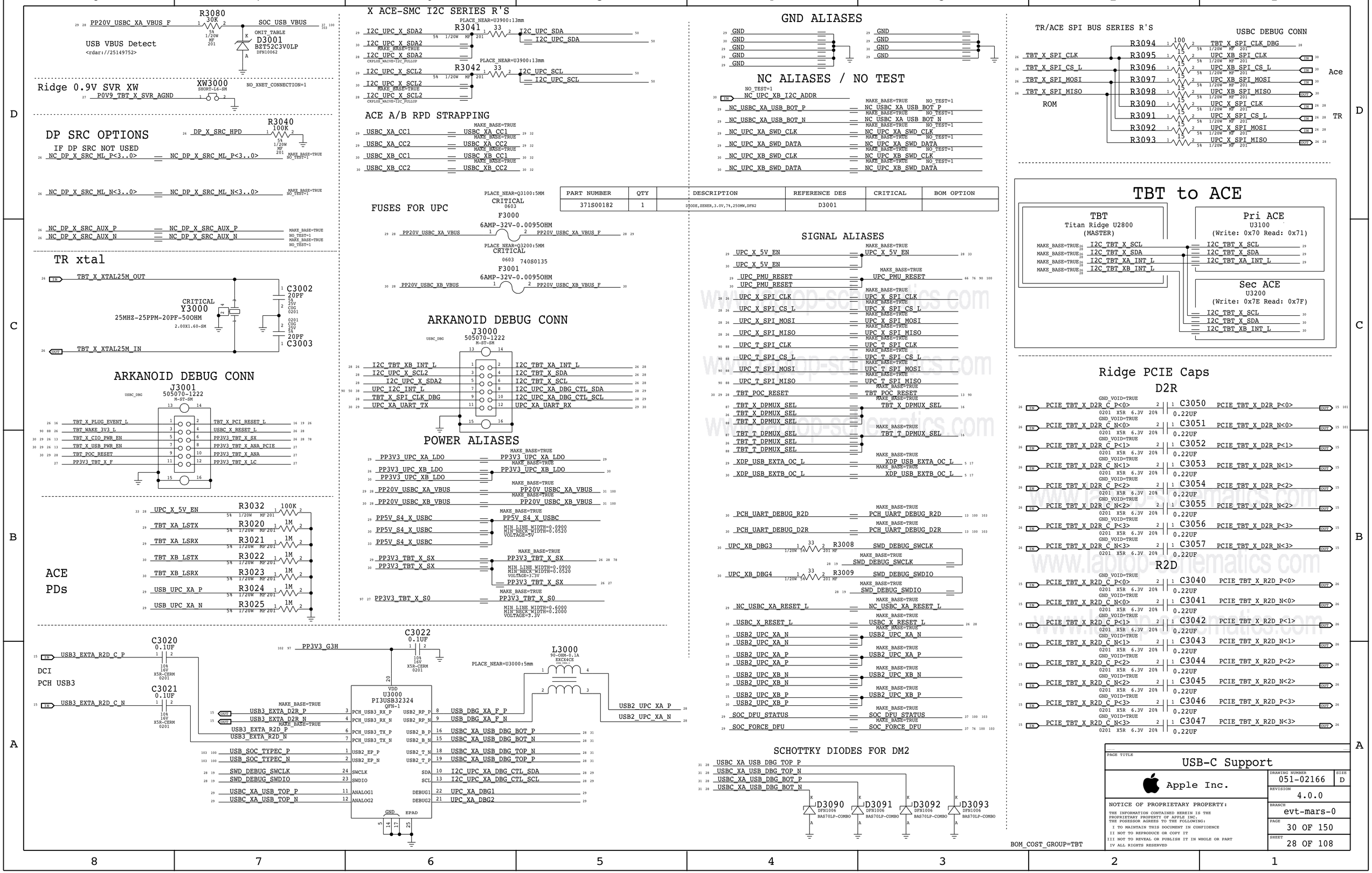

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PAGE TITLE: USB-C Support

Apple Inc.

DRAWING NUMBER: 051-02166 SIZE: D

REVISION: 4.0.0

BRANCH: evt-mars-0

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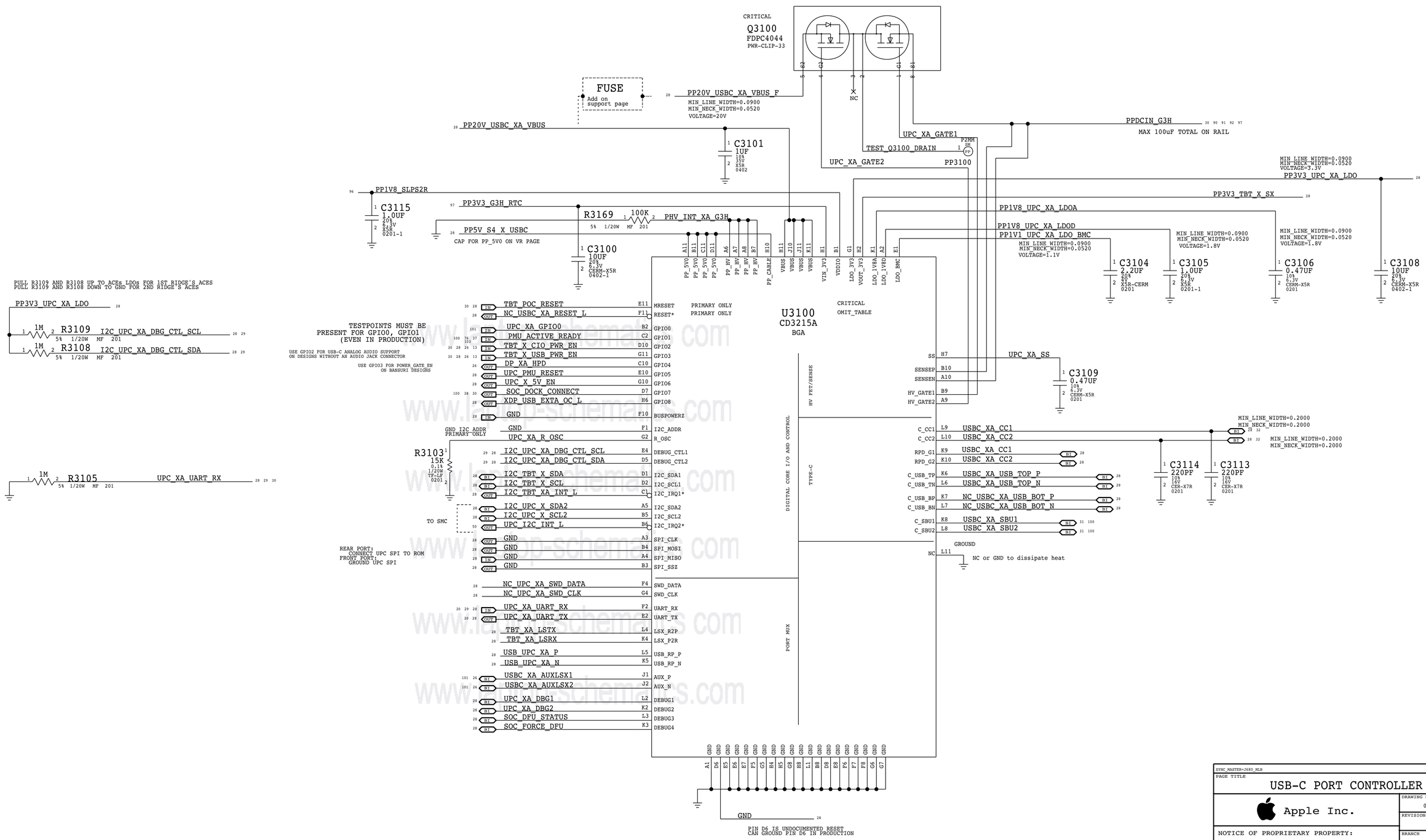
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

SYNC_MASTER=J680_MLB SYNC_DATE=03/30/2017

PAGE TITLE

USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER	051-02166
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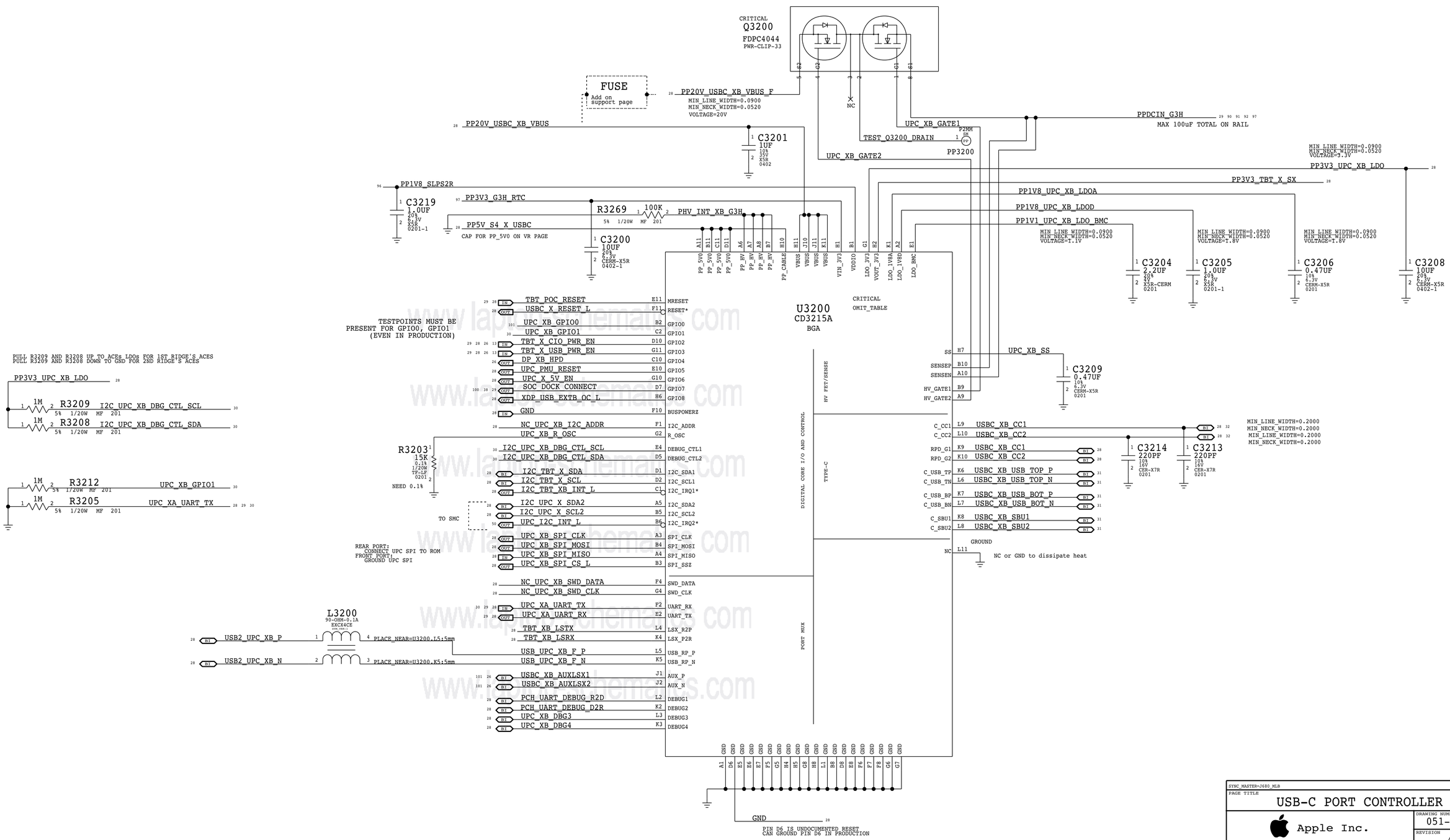
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

SYNC_MASTER=J680_MLB SYNC_DATE=03/30/2017

PAGE TITLE

USB-C PORT CONTROLLER B

Apple Inc.

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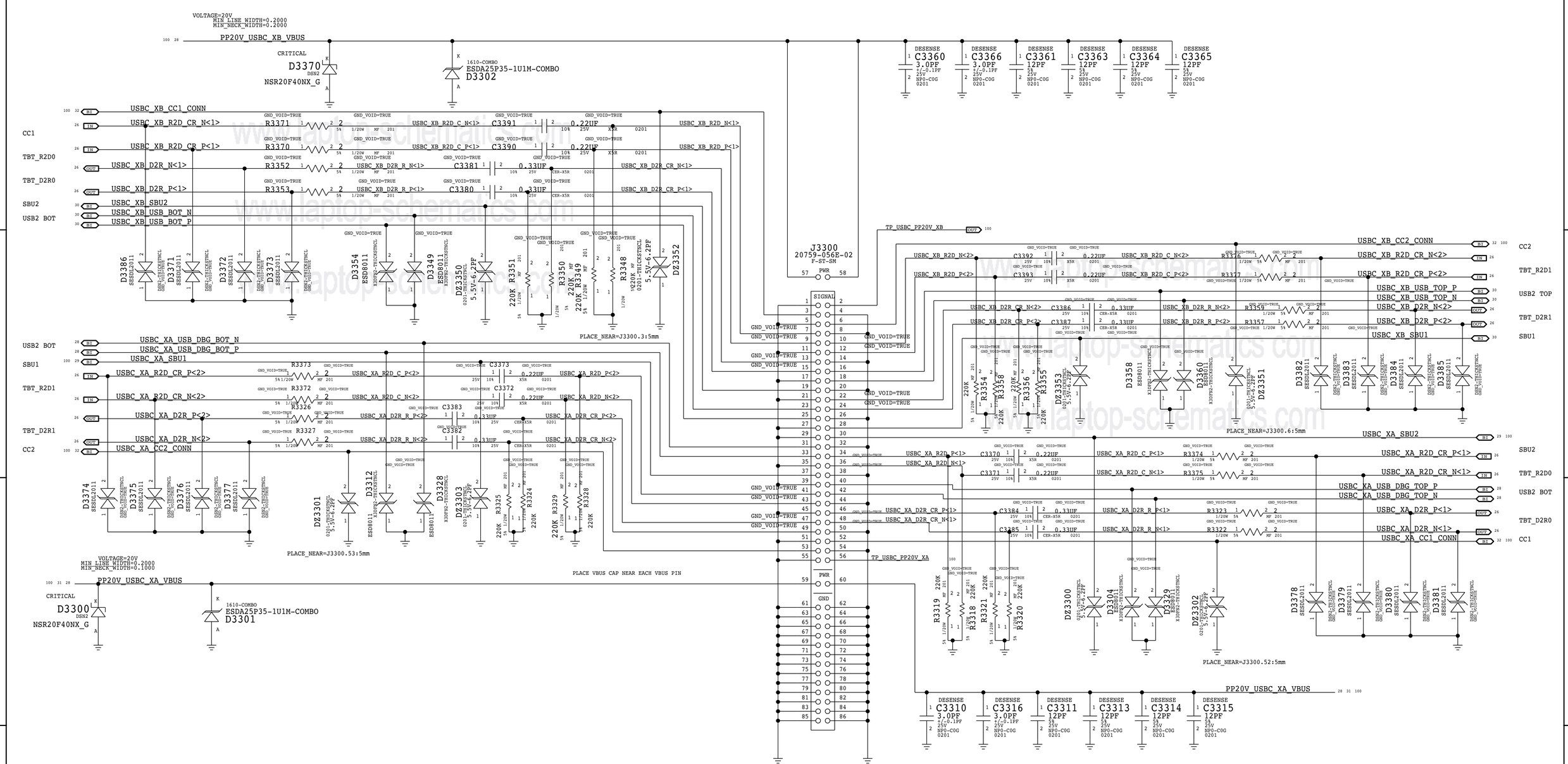

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D

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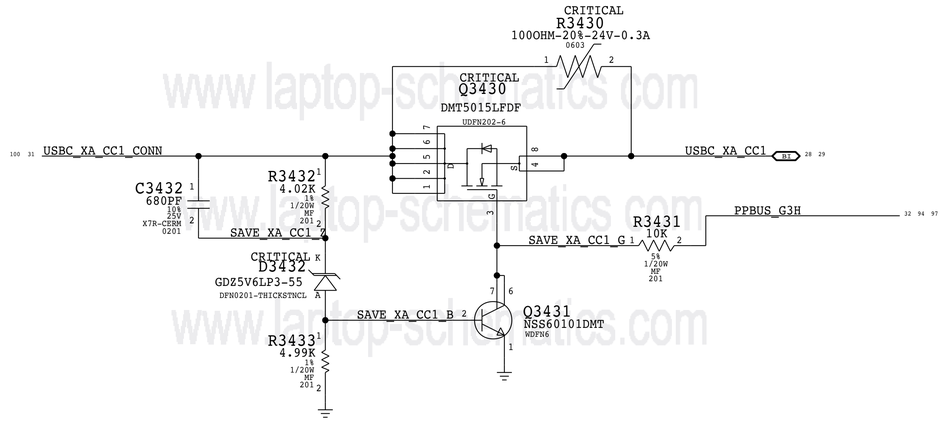
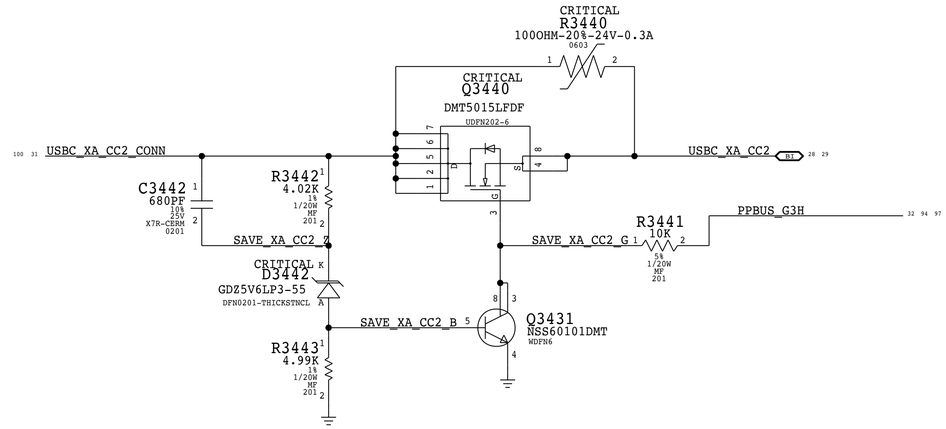
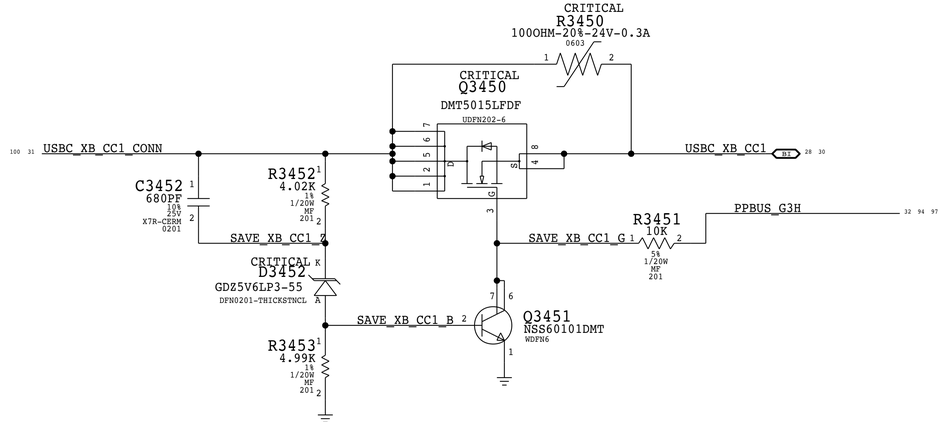
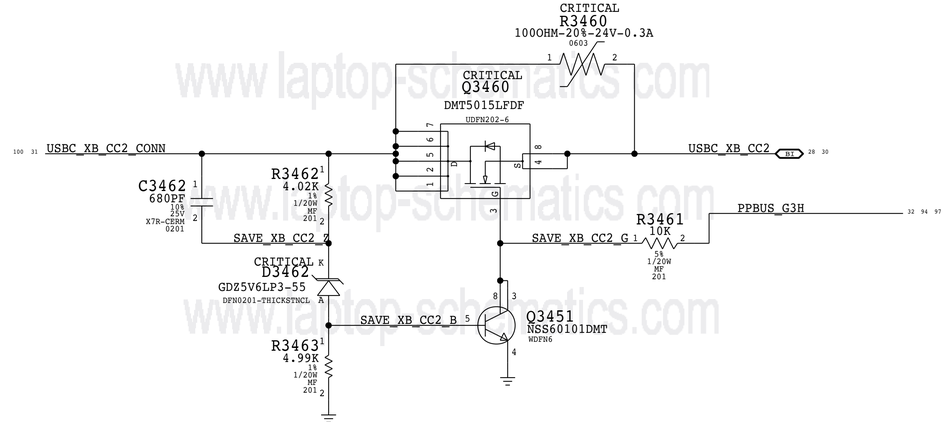
XA CC Protection





XB CC Protection





BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC X Connector Support

Apple Inc.

DRAWING NUMBER 051-02166
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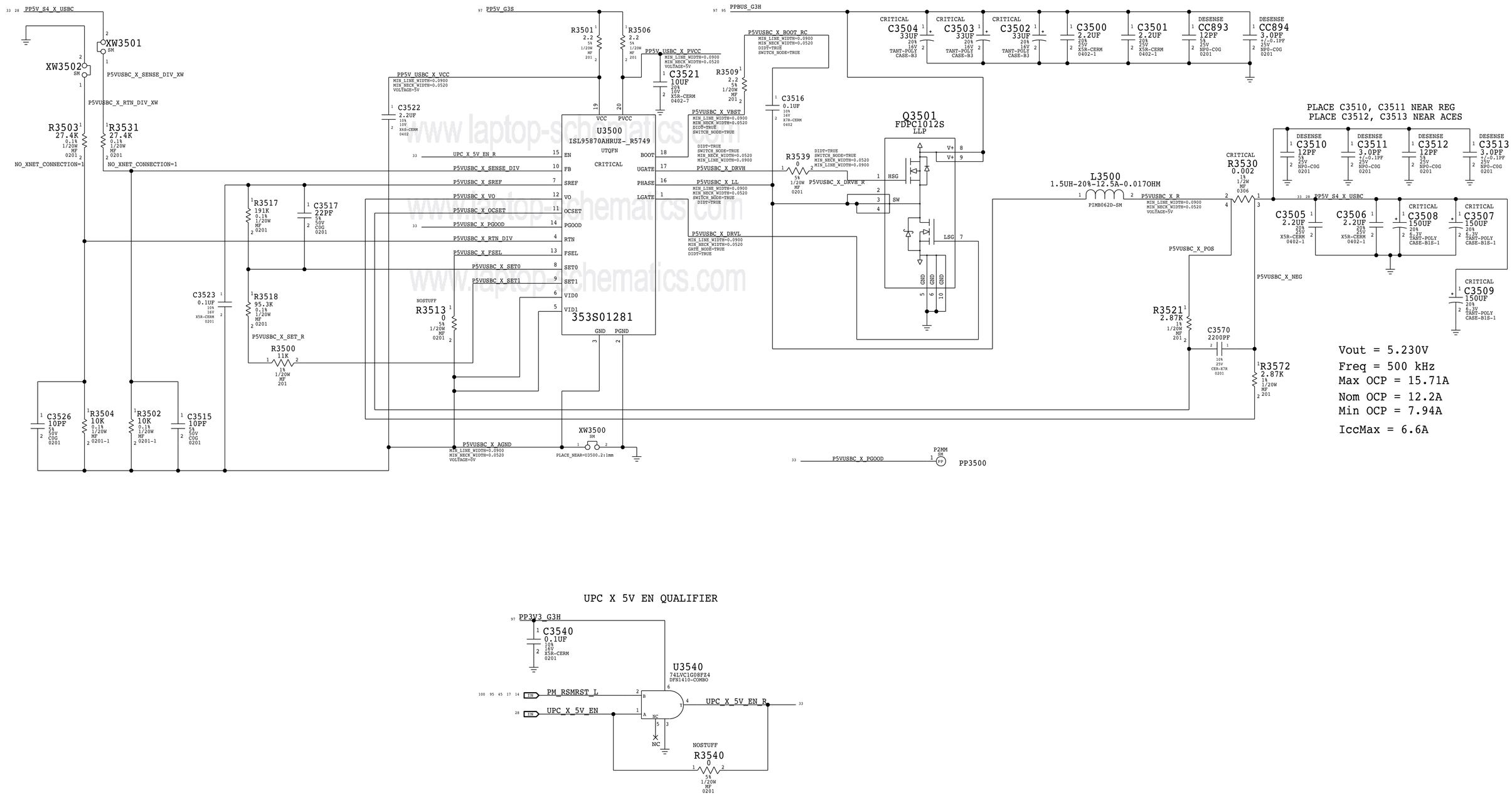

UPC X 5V EN QUALIFIER

BOM_COST_GROUP=USB-C

PAGE TITLE

TBT 5V REGULATOR

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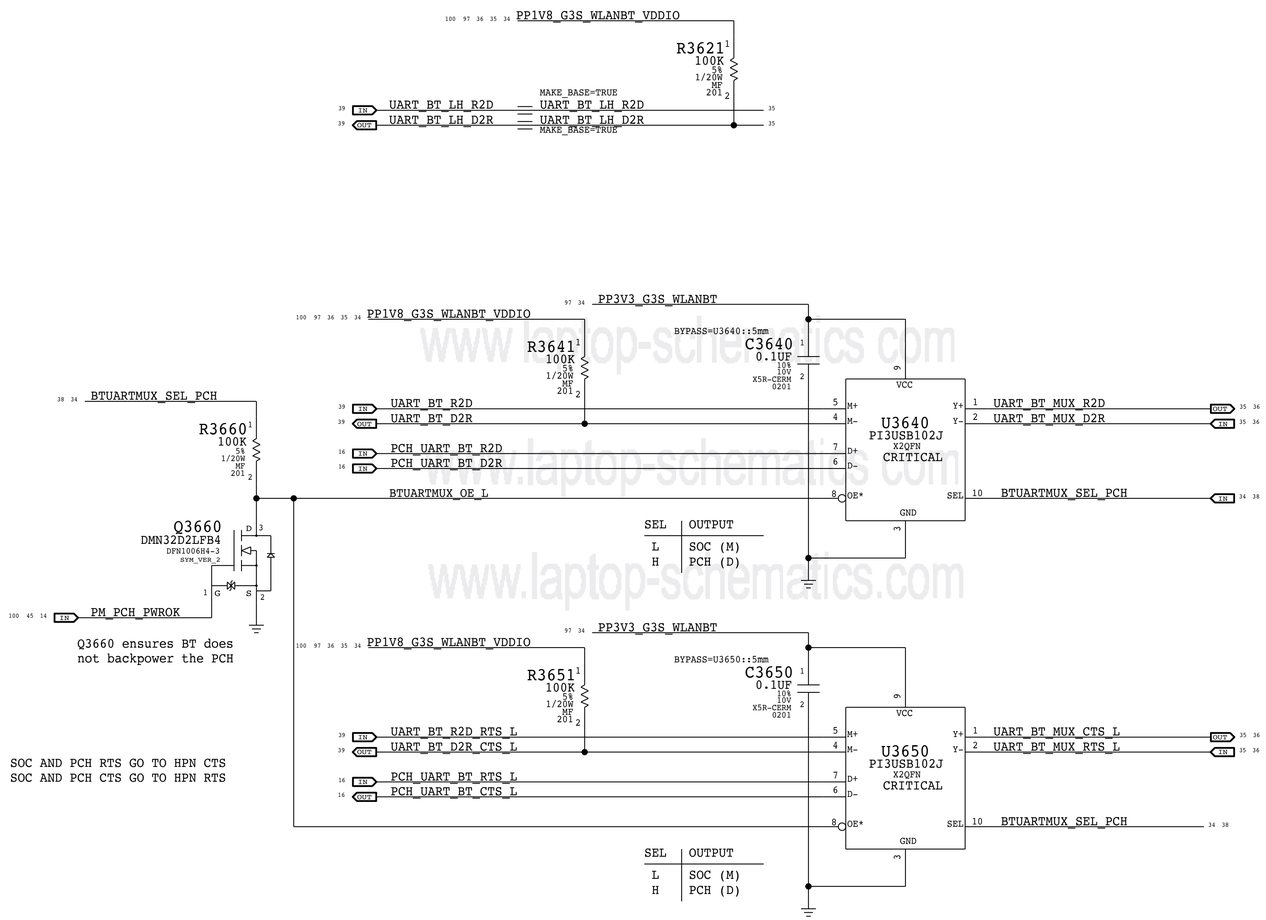
Software	I2S_SEL	UART_SEL	I2S I/F	UART I/F
Gen1 (macOS)	0	1	UART (PCH)	UART (PCH)
Gen1 (Bootcamp)	1	1	I2S (PCH)	UART (PCH)
Gen2	X	0	X	UART (SOC)



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J132_JACK SYNC_DATE=05/30/2017

PAGE TITLE

WIFI/BT: Support

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D

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BRANCH evt-mars-0

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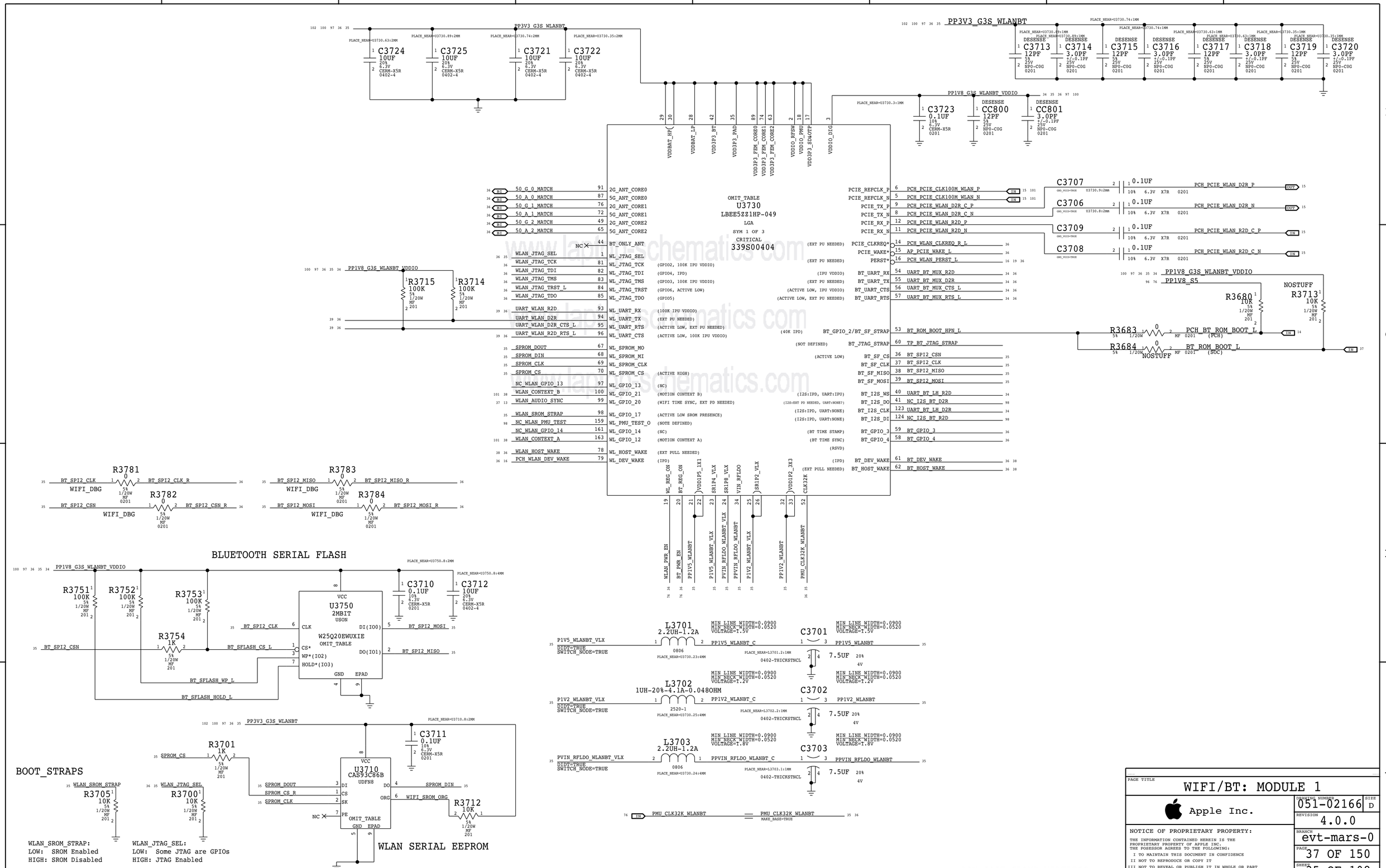
PP3V3_G3S_WLANBT
C3724 10UF 20% 6.3V CERM-X5R 0402-4
C3725 10UF 20% 6.3V CERM-X5R 0402-4
C3721 10UF 20% 6.3V CERM-X5R 0402-4
C3722 10UF 20% 6.3V CERM-X5R 0402-4
C3713 12PF 5% 25V NP0-C0G 0201
C3714 3.0PF ±0.1PF 25V NP0-C0G 0201
C3715 12PF 5% 25V NP0-C0G 0201
C3716 3.0PF ±0.1PF 25V NP0-C0G 0201
C3717 12PF 5% 25V NP0-C0G 0201
C3718 3.0PF ±0.1PF 25V NP0-C0G 0201
C3719 12PF 5% 25V NP0-C0G 0201
C3720 3.0PF ±0.1PF 25V NP0-C0G 0201
PP1V8_G3S_WLANBT_VDDIO
C3723 0.1UF 10% 6.3V CERM-X5R 0201
CC800 12PF 5% 25V NP0-C0G 0201
CC801 3.0PF ±0.1PF 25V NP0-C0G 0201
OMIT_TABLE
U3730
LBEE5ZZ1HP-049
LGA
SYM 1 OF 3
CRITICAL
339S00404
50_G_0_MATCH
50_A_0_MATCH
50_G_1_MATCH
50_A_1_MATCH
50_G_2_MATCH
50_A_2_MATCH
WLAN_JTAG_SEL
WLAN_JTAG_TCK
WLAN_JTAG_TDI
WLAN_JTAG_TMS
WLAN_JTAG_TRST_L
WLAN_JTAG_TDO
UART_WLAN_R2D
UART_WLAN_D2R
UART_WLAN_D2R_CTS_L
UART_WLAN_R2D_RTS_L
SPROM_DOUT
SPROM_DIN
SPROM_CLK
SPROM_CS
NC_WLAN_GPIO_13
WLAN_CONTEXT_B
WLAN_AUDIO_SYNC
WLAN_SROM_STRAP
NC_WLAN_PMU_TEST
NC_WLAN_GPIO_14
WLAN_CONTEXT_A
WLAN_HOST_WAKE
PCH_WLAN_DEV_WAKE
PCIE_REFCLK_P
PCIE_REFCLK_N
PCIE_TX_P
PCIE_TX_N
PCIE_RX_P
PCIE_RX_N
PCIE_CLKREQ*
PCIE_WAKE*
PERST*
BT_UART_RX
BT_UART_TX
BT_UART_CTS
BT_UART_RTS
BT_GPIO_2/BT_SF_STRAP
BT_JTAG_STRAP
BT_SF_CS
BT_SF_CLK
BT_SF_MISO
BT_SF_MOSI
BT_I2S_WS
BT_I2S_DO
BT_I2S_CLK
BT_I2S_DI
BT_GPIO_3
BT_GPIO_4
BT_DEV_WAKE
BT_HOST_WAKE
PCH_PCIE_CLK100M_WLAN_P
PCH_PCIE_CLK100M_WLAN_N
PCH_PCIE_WLAN_D2R_C_P
PCH_PCIE_WLAN_D2R_C_N
PCH_PCIE_WLAN_R2D_P
PCH_PCIE_WLAN_R2D_N
PCH_WLAN_CLKREQ_R_L
AP_PCIE_WAKE_L
PCH_WLAN_PERST_L
C3707 0.1UF 10% 6.3V X7R 0201
C3706 0.1UF 10% 6.3V X7R 0201
C3709 0.1UF 10% 6.3V X7R 0201
C3708 0.1UF 10% 6.3V X7R 0201
PCH_PCIE_WLAN_D2R_P
PCH_PCIE_WLAN_D2R_N
PCH_PCIE_WLAN_R2D_C_P
PCH_PCIE_WLAN_R2D_C_N
PP1V8_S5
R3680 10K 5% 1/20W MF 201
R3713 10K 5% 1/20W MF 201
NOSTUFF
R3683 0 5% 1/20W MF 0201
R3684 0 5% 1/20W MF 0201
PCH_BT_ROM_BOOT_L (PCH)
BT_ROM_BOOT_L (SOC)
R3715 100K 5% 1/20W MF 201
R3714 100K 5% 1/20W MF 201
R3781 0 5% 1/20W MF 0201
R3782 0 5% 1/20W MF 0201
R3783 0 5% 1/20W MF 0201
R3784 0 5% 1/20W MF 0201
WIFI_DBG
BT_SPI2_CLK_R
BT_SPI2_CSN_R
BT_SPI2_MISO_R
BT_SPI2_MOSI_R
BLUETOOTH SERIAL FLASH
R3751 100K 5% 1/20W MF 201
R3752 100K 5% 1/20W MF 201
R3753 100K 5% 1/20W MF 201
R3754 1K 5% 1/20W MF 201
C3710 0.1UF 10% 6.3V CERM-X5R 0201
C3712 10UF 20% 6.3V CERM-X5R 0402-4
U3750
2MBIT
USON
W25Q20EWUXIE
OMIT_TABLE
BT_SPI2_CLK
BT_SPI2_CSN
BT_SPI2_MOSI
BT_SPI2_MISO
BT_SFLASH_CS_L
BT_SFLASH_WP_L
BT_SFLASH_HOLD_L
BOOT_STRAPS
R3701 1K 5% 1/20W MF 201
R3705 10K 5% 1/20W MF 201
R3700 10K 5% 1/20W MF 201
C3711 0.1UF 10% 6.3V CERM-X5R 0201
U3710
CAS93C86B
UDFN8
SPROM_CS
SPROM_DOUT
SPROM_CS_R
SPROM_CLK
SPROM_DIN
WIFI_SROM_ORG
R3712 10K 5% 1/20W MF 201
WLAN_SROM_STRAP:
LOW: SROM Enabled
HIGH: SROM Disabled
WLAN_JTAG_SEL:
LOW: Some JTAG are GPIOs
HIGH: JTAG Enabled
WLAN SERIAL EEPROM
L3701 2.2UH-1.2A 0806
C3701 7.5UF 20% 4V 0402-THICKSTNCL
L3702 1UH-20%-4.1A-0.048OHM 2520-1
C3702 7.5UF 20% 4V
L3703 2.2UH-1.2A 0806
C3703 7.5UF 20% 4V
P1V5_WLANBT_VLX
PP1V5_WLANBT_C
PP1V5_WLANBT
P1V2_WLANBT_VLX
PP1V2_WLANBT_C
PP1V2_WLANBT
PVIN_RFLDO_WLANBT_VLX
PPVIN_RFLDO_WLANBT_C
PPVIN_RFLDO_WLANBT
PMU_CLK32K_WLANBT
BOM_COST_GROUP=WIRELESS
PAGE TITLE
WIFI/BT: MODULE 1
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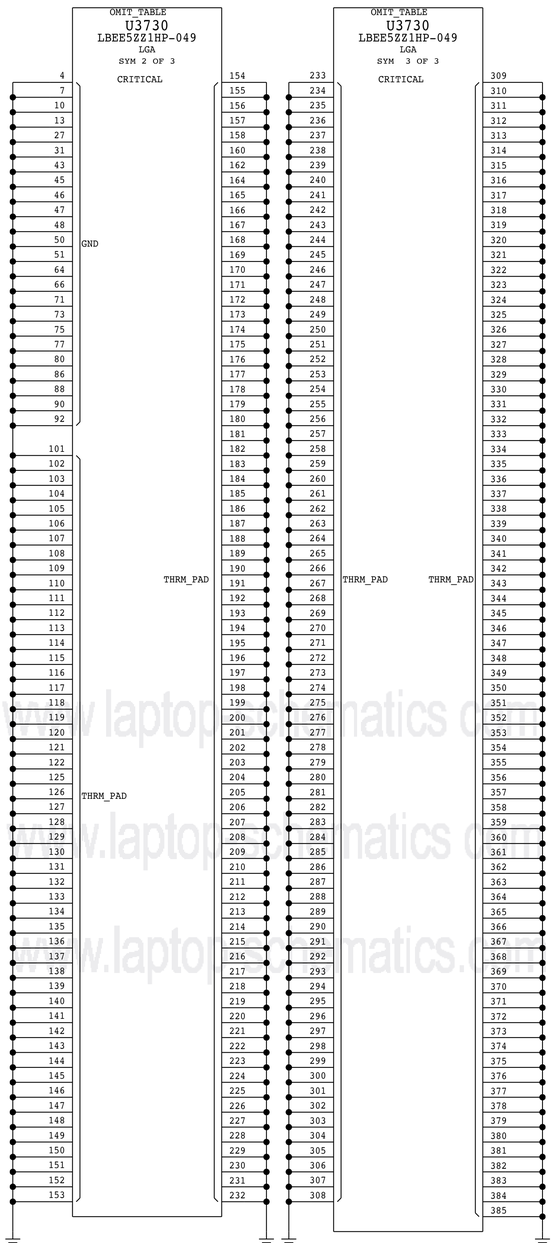

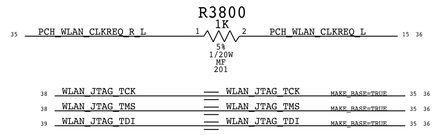

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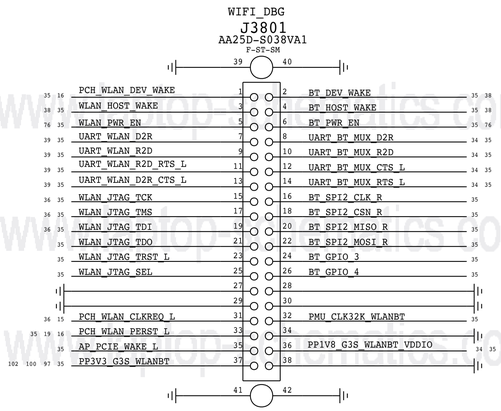

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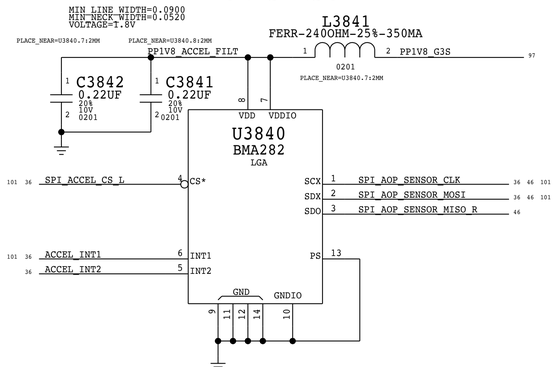
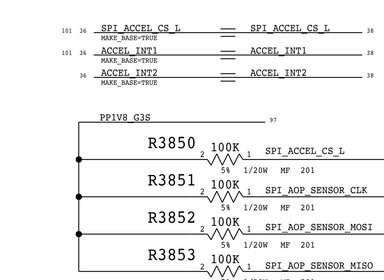
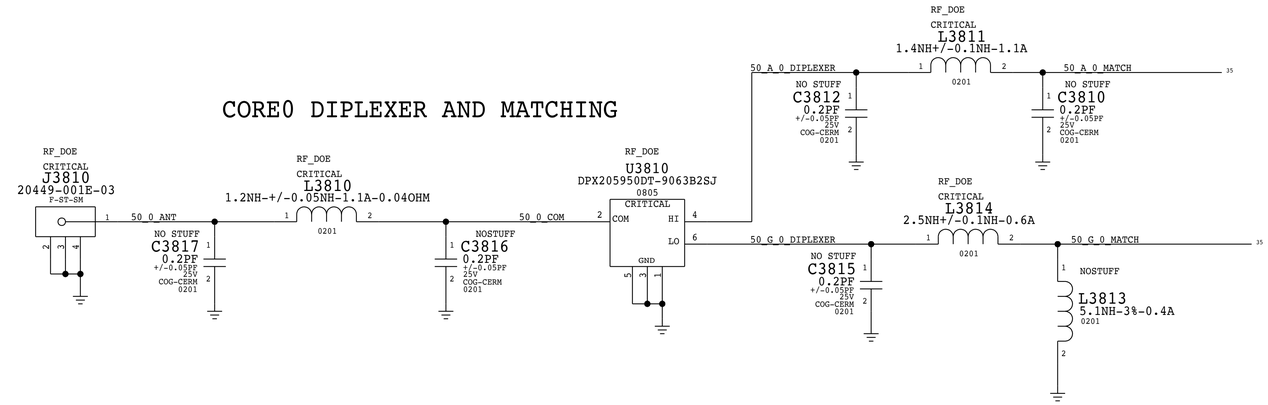




CORE0 DIPLEXER AND MATCHING



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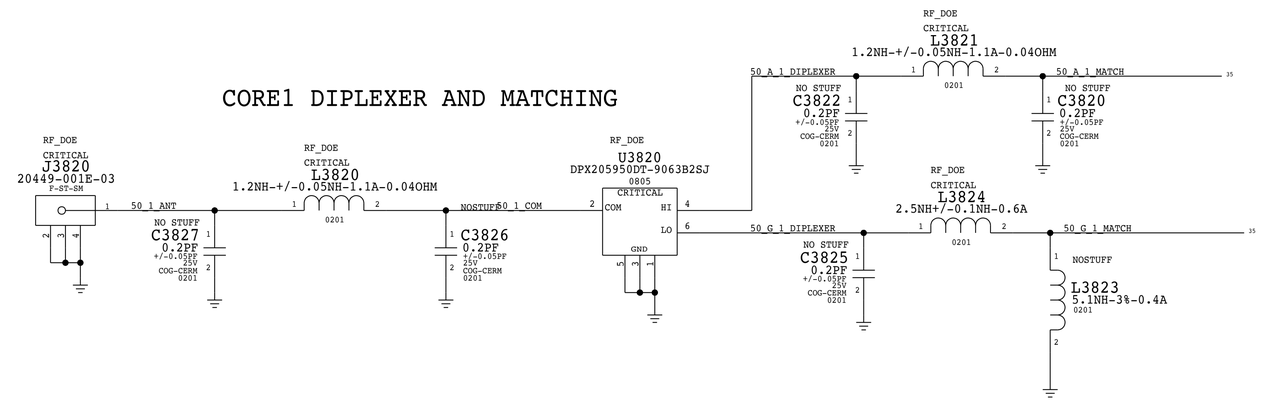
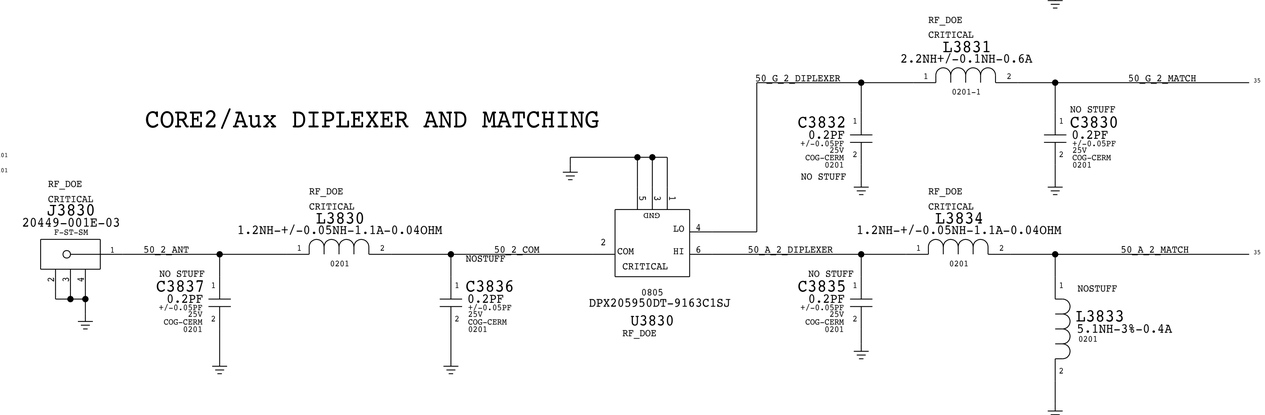


CORE2/Aux DIPLEXER AND MATCHING



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PAGE TITLE

WIFI/BT: MODULE 2

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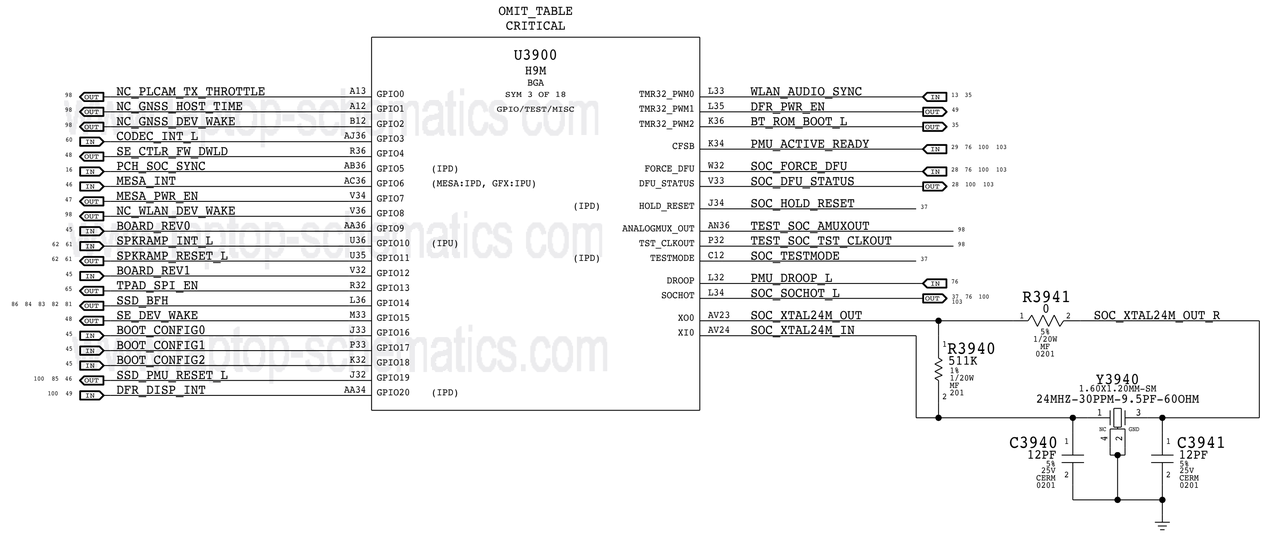
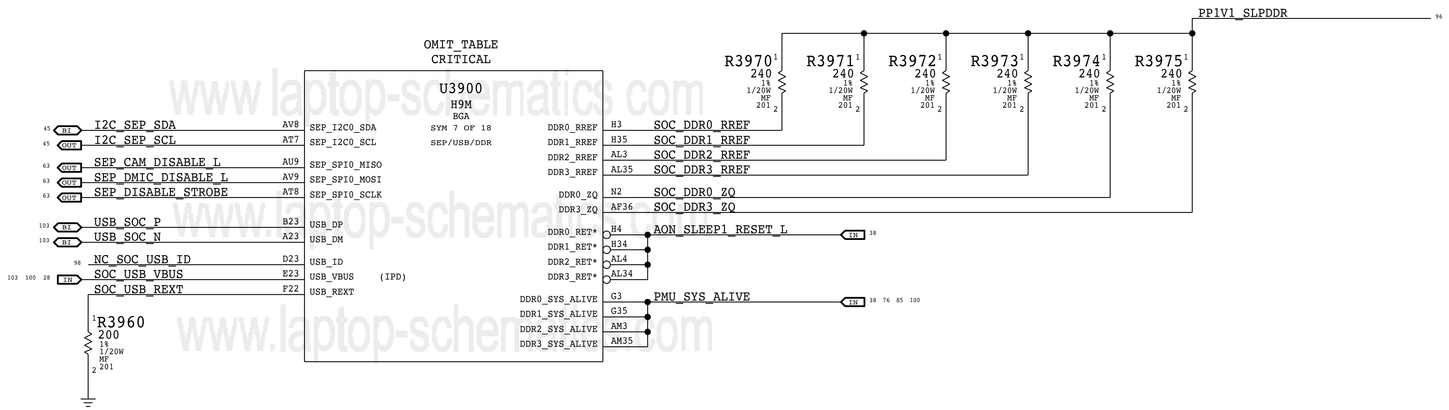
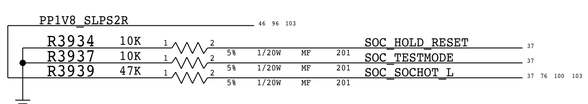
Note 1) IPU represents SW configured state, not HW default







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	REVISION: 4.0.0
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AOP

WLAN_CONTEXT_A	D3	AOP_FUNC[0]		AOP_PDM_CLK0	P6	PDM_DMIC_CLK0_R	46
WLAN_CONTEXT_B	F4	AOP_FUNC[1]		AOP_PDM_CLK1	K2	PDM_DMIC_CLK1_R	46
ACCEL_INT1	M6	AOP_FUNC[2]	(IPD)	AOP_PDM_CLK2 (IPU)	J6	TP_SMC_FIXTURE_MODE_L	98 100
ACCEL_INT2	D4	AOP_FUNC[3]	(IPD)	AOP_PDM_CLK3 (IPU)	L6	NC_PLCAM_PROX_INT_L	98
BTUARTMUX_SEL_PCH	F3	AOP_FUNC[4]		AOP_PDM_CLK4 (IPU)	L5	NC_PLCAM_ROMEO_B2B_DETECT	98
SOC_PERST_L	K6	AOP_FUNC[5]					
NC_ALTIMETER_INT	E4	AOP_FUNC[6]	(IPD)	AOP_PDM_DATA0 (IPD)	J5	PDM_DMIC_DATA0	63
SPI_ACCEL_CS_L	J3	AOP_FUNC[7]		AOP_PDM_DATA1 (IPD)	K4	PDM_DMIC_DATA1	63
NC_SPI_ALTIMETER_CS_L	H6	AOP_FUNC[8]		AOP_SPI_MOSI	D2	SPI_AOP_SENSOR_MOSI_R	46
				AOP_SPI_SCLK	F2	SPI_AOP_SENSOR_CLK_R	46
NC_I2C_AOP_SCL	N6	AOP_I2C0_SCL		AOP_SPI_MISO	E2	SPI_AOP_SENSOR_MISO	36 46 101
NC_I2C_AOP_SDA	G5	AOP_I2C0_SDA					

OMIT_TABLE
CRITICAL

U3900
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AON

DFR_TOUCH_INT_L	AL6	AON_GPIO0		JTAG_TCK (IPU)	AK6	SWD_SOC_SWCLK	19 100 103
CPU_SMC_THRMTRIP_L	AE6	AON_GPIO1	(IPU)	JTAG_TMS (IPU)	AN5	SWD_SOC_SWDIO	19 100 103
NC_SMC_GFX_SELF_THROTTLE	AT5	AON_GPIO2	(IPD)	JTAG_TDI (IPU)	AH6	DEBUG_JTAG_SOC_TDI	100 103
NC_SMC_TOPBLK_SWP_L	AN4	AON_GPIO3		JTAG_TDO	AP4	DEBUG_JTAG_SOC_TDO	100 103
XDP_PRESENT_L	AK4	AON_GPIO4		JTAG_TRST* (IPD)	AJ6	TP_JTAG_SOC_TRST_L	100
CODEC_RESET_L	AV5	AON_GPIO5		JTAG_SEL	AC6	SOC_JTAG_SEL (DAP=0, TAP=1)	38
BT_DEV_WAKE	AR3	AON_GPIO6					
NC_PCIEDN_WAKE_L	AG6	AON_GPIO7	(IPU)	DOCK_CONNECT	AN2	SOC_DOCK_CONNECT	29 30 38 100
NC_ENET_LOW_PWR	AU5	AON_GPIO8					
TPAD_SPI_INT_L	AP2	AON_GPIO9		AON_SWD0_TMS	AJ4	WLAN_JTAG_TMS	36
NC_SDCONN_STATE_CHANGE_L	AR4	AON_GPIO10	(IPU)	AON_SWD1_TMS (IPU)	AH4	NC_MESA_MENUKEY_L	98
NC_ENET_MEDIA_SENSE	AN3	AON_GPIO11	(IPD)	AON_SWD01_TCK	AJ2	WLAN_JTAG_TCK	36
PMU_INT_L	AT6	AON_GPIO12	(IPU)	WDOG	AJ5	SOC_WDOG	76 100
				AON_SLEEP1_RESET*	AF6	AON_SLEEP1_RESET_L	37
		AON_SPMI_SCLK					
		AON_SPMI_SDATA					
SPMI_CLK R4036 20 1/20W MF 201 (PLACE_NEAR=U3900.AD6:5MM, PLACE_NEAR=U7800.M7:5MM)	AD6	SPMI_CLK_R					
SPMI_DATA R4037 20 1/20W MF 201	AR2	SPMI_DATA_R					
PMU_CLK32K_SOC	AR5	RT_CLK32768					
SOC_COLD_RESET_L R4039 4.7K 1/20W MF 201	AK2	COLD_RESET*					
	AK3	CFSB_AON					
PMU_COLD_RESET_L							

OMIT_TABLE
CRITICAL

U3900
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SMC

ESPI_IO<0> R4050 20 1/20W MF 201 (PLACE_NEAR=U3900.U2:5MM)	V2	SMC_ESPI_IO0		SMC_GPIO0	Y4	CODEC_WAKE_L	40
ESPI_IO<1> R4051 20 1/20W MF 201 (PLACE_NEAR=U3900.V2:5MM)	U3	SMC_ESPI_IO1		SMC_GPIO1 (IPD)	Y8	BT_HOST_WAKE	35 36
ESPI_IO<2> R4052 20 1/20W MF 201 (PLACE_NEAR=U3900.U3:5MM)	U4	SMC_ESPI_IO2		SMC_GPIO2 (IPD)	Y5	WLAN_HOST_WAKE	35 36
ESPI_IO<3> R4053 20 1/20W MF 201 (PLACE_NEAR=U3900.V4:5MM)	V8	SMC_ESPI_IO3		SMC_GPIO3	AA2	DP_INT_HPD_MASK	46
ESPI_CLK60M	U2	SMC_ESPI_CLK	(IPD)	SMC_GPIO4	Y7	LID_OPEN_RIGHT	46
ESPI_CS_L	V7	SMC_ESPI_CS*		SMC_GPIO5 (IPD)	Y6	NC_PCC_EVENT	98
ESPI_RESET_L	V6	SMC_ESPI_RESET*	(IPD)	SMC_GPIO6	AB2	NC_TPAD_VIBE_L	98
				SMC_GPIO7	AD5	TPAD_KBD_WAKE_L	46
SMC_PECI_RX	M5	SMC_PECI_IN	(IPD)	SMC_GPIO8	AD2	LID_OPEN_LEFT	46
SMC_PECI_TX	T6	SMC_PECI_OUT		SMC_GPIO9	AB4	NC_SPI_DESCRIPTOR_OVERRIDE_L	98
SMC_PCH_PWROK	W7	PCH_PWROK		SMC_GPIO10 (IPU)	AC2	NC_DISP_GCON_INT_L	98
SMC_PCH_SYS_PWROK	W8	SYS_PWROK		SMC_GPIO11	AC3	NC_SOC_PCH_GCON_INT_L	98
				SMC_GPIO12	AA8	TPAD_ACTUATOR_DISABLE_L	46
SMC_RSMRST_L	W6	RSMRST*		SMC_GPIO13 (IPU)	AB3	TBT_WAKE_L	90
SMC_SYSRST_L	W4	SYS_RESET*		SMC_GPIO14 (IPU)	AE2	UPC_I2C_INT_L	28 50 90
PM_SLP_S0_L	AA4	SLP_S0B		SMC_GPIO15 (IPD)	L4	DP_INT_HPD_L	46
SMC_PROCHOT_L	R5	PROCHOT*					
PMU_SYS_ALIVE	AA6	SYS_ALIVE					
				SMC_ADC0	AG2	SMC_CPU_HS_ISENSE	58
				SMC_ADC1	AC4	SMC_PBUS_VSENSE	58
				SMC_ADC2	AH3	SMC_BMON_ISENSE	58
				SMC_ADC3	AD4	SMC_DCIN_ISENSE	58
				SMC_ADC4	AB6	SMC_DCIN_VSENSE	58
				SMC_ADC5	AH2	SMC_PP3V3_WLANBT_ISENSE	58
				SMC_ADC6	AG4	SMC_PP1V8_WLANBT_ISENSE	58
				SMC_ADC7	AC5	SMC_CALPE_ISENSE	58
I2C_UPC_SCL	M3	SMC_I2C0_SCL					
I2C_UPC_SDA	J4	SMC_I2C0_SDA					
I2C_SNS0_S0_SCL	N4	SMC_I2C1_SCL					
I2C_SNS0_S0_SDA	P4	SMC_I2C1_SDA					
I2C_SNS1_S0_SCL	U5	SMC_I2C2_SCL					
I2C_SNS1_S0_SDA	M2	SMC_I2C2_SDA					
I2C_DISP_SCL	U6	SMC_I2C3_SCL					
I2C_DISP_SDA	R4	SMC_I2C3_SDA					
I2C_PWR_SCL	P3	SMC_I2C4_SCL					
I2C_PWR_SDA	T4	SMC_I2C4_SDA					
I2C_SNS_G3S_SCL	R2	SMC_I2C5_SCL					
I2C_SNS_G3S_SDA	P2	SMC_I2C5_SDA					
I2C_SSD_SCL	R3	SMC_I2C6_SCL					
I2C_SSD_SDA	T2	SMC_I2C6_SDA					
				REFP_ADC	AF4	PP1V25_SLPS2R_SMC_AVREF	45
				REFM_ADC	AG3	GND_SMC_AVSS (PLACE_NEAR=U3900.AF3:4MM)	
				SMC_PWM0	J2	SMC_FAN_0_PWM	58
				SMC_TACH0	L3	SMC_FAN_0_TACH	58
				SMC_PWM1	R6	SMC_FAN_1_PWM	58
				SMC_TACH1	L2	SMC_FAN_1_TACH	58
				SMC_PWM2	M4	NC_SMC_LED_ONEWIRE	98
			(IPU)	SMC_UART0_RXD	V4	SMC_DEBUGPRT_RX	90 100 103
				SMC_UART0_TXD	V5	SMC_DEBUGPRT_TX	90 100 103
				SWD_OUT0_TCK	AE3	SSD0_SWCLK	46 81 82 83 84 86
				SWD_OUT0_TMS	AA5	SSD0_SWDIO	46 81 82 83 84 86
				SWD_OUT1_TCK	AF2	NC_SSD1_SWCLK_UART_R2D	98
				SWD_OUT1_TMS	AA7	NC_SSD1_SWDIO_UART_D2R	98

XW4089
SM
1 2

PP1V8_S5 (13 14 15 16 96)

R4046	10K	SOC_JTAG_SEL	38
R4047	100K	SOC_DOCK_CONNECT	29 30 38 100
R4054	100K	ESPI_IO<0>	13 19 38
R4055	100K	ESPI_IO<1>	13 19 38
R4056	100K	ESPI_IO<2>	13 19 38
R4057	100K	ESPI_IO<3>	13 19 38
R4059	100K	ESPI_CS_L	13 19 38

5% 1/20W MF 201

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SYNC_MASTER=T290_BIGSUR SYNC_DATE=06/14/2017

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SoC AOP/AON/SMC

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OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 4 OF 18
ISP

MIPI_FTCAM_DATA_P<0>	B27	MIPI0C_DATA0_P		ISP_I2C0_SDA	AF32	I2C_FTCAM_SDA	
MIPI_FTCAM_DATA_N<0>	A27	MIPI0C_DATA0_N		ISP_I2C0_SCL	AH36	I2C_FTCAM_SCL	
GND	B25	MIPI0C_DATA1_P		ISP_I2C1_SDA	AB32	NC_I2C_PLCAM_SDA	
GND	A25	MIPI0C_DATA1_N		ISP_I2C1_SCL	AG32	NC_I2C_PLCAM_SCL	
MIPI_FTCAM_CLK_P	B26	MIPI0C_CLK_P		SENSOR0_CLK	AK35	NC_FTCAM_CLK12M_R	
MIPI_FTCAM_CLK_N	A26	MIPI0C_CLK_N		SENSOR0_RST	AK34	NC_FTCAM_RESET_L	
				SENSOR0_ISTRB	AJ33	DFR_TOUCH_RESET_L	
GND	B28	MIPI1C_DATA0_P		SENSOR1_CLK	AD33	NC_PLCAM_RX_CLK12M_R	
GND	A28	MIPI1C_DATA0_N		SENSOR1_RST	AC32	NC_PLCAM_RX_RESET_L	
GND	B30	MIPI1C_DATA1_P		SENSOR1_ISTRB	AC34	DFR_DISP_RESET_L	
GND	A30	MIPI1C_DATA1_N		SENSOR2_CLK	AD32	NC_PLCAM_TX_CLK12M_R	
GND	B29	MIPI1C_CLK_P		SENSOR2_RST	AJ32	NC_PLCAM_TX_RESET_L	
GND	A29	MIPI1C_CLK_N		(IPD) SENSOR_INT	AA33	NC_PLCAM_TX_INT	
MIPI_DFR_DATA_P	B33	MIPID_DATA0_P					
MIPI_DFR_DATA_N	A33	MIPID_DATA0_N		(IPD) DISP_TE	H32	DFR_DISP_TE	
MIPI_DFR_CLK_P	B32	MIPID_CLK_P		DISP_VSYNC	T36	BOARD_REV2	
MIPI_DFR_CLK_N	A32	MIPID_CLK_N		CLK32K_OUT	AK33	DFR_TOUCH_CLK32K_RESET_L	
SOC_MIPI0C_REXT	F23	MIPI0C_REXT					
SOC_MIPI1C_REXT	F26	MIPI1C_REXT					
SOC_MIPID_REXT	F27	MIPID_REXT					

R4100 4.02K 1% 1/20W MF 201
R4101 4.02K 1% 1/20W MF 201
R4102 4.02K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 2 OF 18
I2C/UART/SPI/I2S

I2C_SPKRAMP_L_SDA	AE35	I2C0_SDA		SPI0_MISO	AR9	SPI_SOCROM_MISO	
I2C_SPKRAMP_L_SCL	AD35	I2C0_SCL		SPI0_MOSI	AR7	SPI_SOCROM_MOSI_R	
I2C_SPKRAMP_R_SDA	AF34	I2C1_SDA		SPI0_SCLK	AU7	SPI_SOCROM_CLK_R	
I2C_SPKRAMP_R_SCL	AG35	I2C1_SCL		SPI0_SSIN	AT9	SPI_SOCROM_CS_L	
I2C_CODEC_SDA	M34	I2C2_SDA		(IPU) SPI1_MISO	P36	SPI_TPAD_MISO	
I2C_CODEC_SCL	R33	I2C2_SCL		SPI1_MOSI	N34	SPI_TPAD_MOSI_R	
I2C_ALS_SDA	Y32	I2C3_SDA		SPI1_SCLK	P35	SPI_TPAD_CLK_R	
I2C_ALS_SCL	AE34	I2C3_SCL		SPI1_SSIN	T32	SPI_TPAD_CS_L	
I2C_DFR_SDA	T34	I2C4_SDA		SPI2_MISO	A19	SPI_MESA_MISO	
I2C_DFR_SCL	U32	I2C4_SCL		SPI2_MOSI	A20	SPI_MESA_MOSI_R	
NC_I2C_SOC_5_SDA	R35	I2C5_SDA		SPI2_SCLK	C19	SPI_MESA_CLK_R	
NC_I2C_SOC_5_SCL	U33	I2C5_SCL		SPI2_SSIN	A18	WLAN_JTAG_TDI	
SPKR_ID1	P34	I2C6_SDA	(IPU)	SPI3_MISO	C17	SPI_DFR_MISO	
SPKR_ID0	R34	I2C6_SCL	(IPU)	SPI3_MOSI	C18	SPI_DFR_MOSI_R	
				SPI3_SCLK	B18	SPI_DFR_CLK_R	
TP_SOC_DEBUGPRT_RX	Y33	UART0_RXD	(IPU)	SPI3_SSIN	A17	SPI_DFR_CS_L	
TP_SOC_DEBUGPRT_TX	Y34	UART0_TXD		(IPD) I2S0_DIN	AC33	I2S_SPKRAMP_L_D2R	
UART_SE_D2R	B15	UART1_RXD		I2S0_DOUT	AG34	I2S_SPKRAMP_L_R2D_R	
UART_SE_R2D	A15	UART1_TXD		I2S0_BCLK	AA32	I2S_SPKRAMP_L_BCLK_R	
UART_SE_D2R_CTS_L	C15	UART1_CTS*		I2S0_LRCK	AG33	I2S_SPKRAMP_L_LRCLK	
UART_SE_R2D_RTS_L	D15	UART1_RTS*		I2S0_MCK	AR35	NC_DFR_TOUCH_RSVD	
UART_BT_D2R	J36	UART2_RXD		(IPD) I2S1_DIN	B20	I2S_SPKRAMP_R_D2R	
UART_BT_R2D	J35	UART2_TXD		I2S1_DOUT	C20	I2S_SPKRAMP_R_R2D_R	
UART_BT_D2R_CTS_L	N32	UART2_CTS*		I2S1_BCLK	C21	I2S_SPKRAMP_R_BCLK_R	
UART_BT_R2D_RTS_L	M32	UART2_RTS*		I2S1_LRCK	A21	I2S_SPKRAMP_R_LRCLK	
				I2S1_MCK	D21	NC_PCHROM_SW_EN	
UART_BT_LH_D2R	M36	UART3_RXD		(IPD) I2S2_DIN	AH34	I2S_CODEC_D2R	
UART_BT_LH_R2D	N36	UART3_TXD		I2S2_DOUT	AB34	I2S_CODEC_R2D_R	
NC_UART_GNSS_D2R_CTS_L	M35	UART3_CTS*		I2S2_BCLK	AF33	I2S_CODEC_BCLK_R	
NC_UART_GNSS_R2D_RTS_L	U34	UART3_RTS*		I2S2_LRCK	AH35	I2S_CODEC_LRCLK	
				I2S2_MCK	AR33	NC_I2S_CODEC_MCLK	
UART_WLAN_D2R	B14	UART4_RXD		(IPD) I2S3_DIN	AD36	NC_I2S_HAWKING_D2R	
UART_WLAN_R2D	A14	UART4_TXD		I2S3_DOUT	AB35	NC_I2S_CODEC1_R2D_R	
UART_WLAN_D2R_CTS_L	C14	UART4_CTS*		I2S3_BCLK	AE36	NC_I2S_HAWKING_BCLK_R	
UART_WLAN_R2D_RTS_L	C13	UART4_RTS*		I2S3_LRCK	W34	NC_I2S_HAWKING_LRCLK	
				I2S3_MCK	AG36	NC_I2S_CODEC1_MCLK	

PLACE_NEAR=U3900.AR7:5MM
PLACE_NEAR=U3900.AU7:5MM

R4171 20 5% 1/20W MF 201 SPI_SOCROM_MOSI
R4172 20 5% 1/20W MF 201 SPI_SOCROM_CLK

BOM_COST_GROUP=SOC

SYNC_MASTER=T290_BIGSUR SYNC_DATE=05/26/2017

PAGE TITLE
SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
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SHEET 39 OF 108

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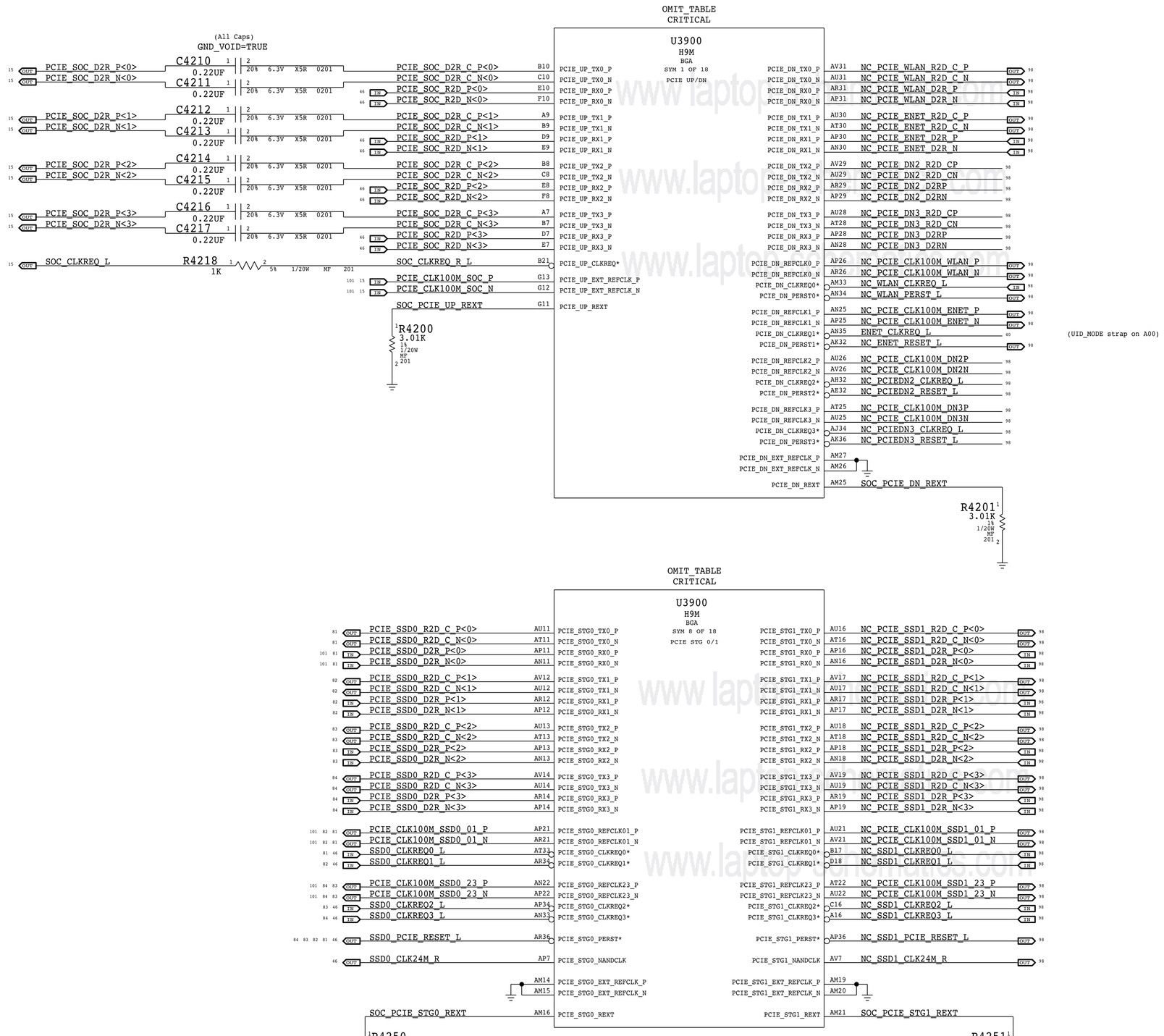

BOM_COST_GROUP=SOC

SYNC_MASTER=T290_BIGSUR SYNC_DATE=03/15/2017

PAGE TITLE

SoC PCIe

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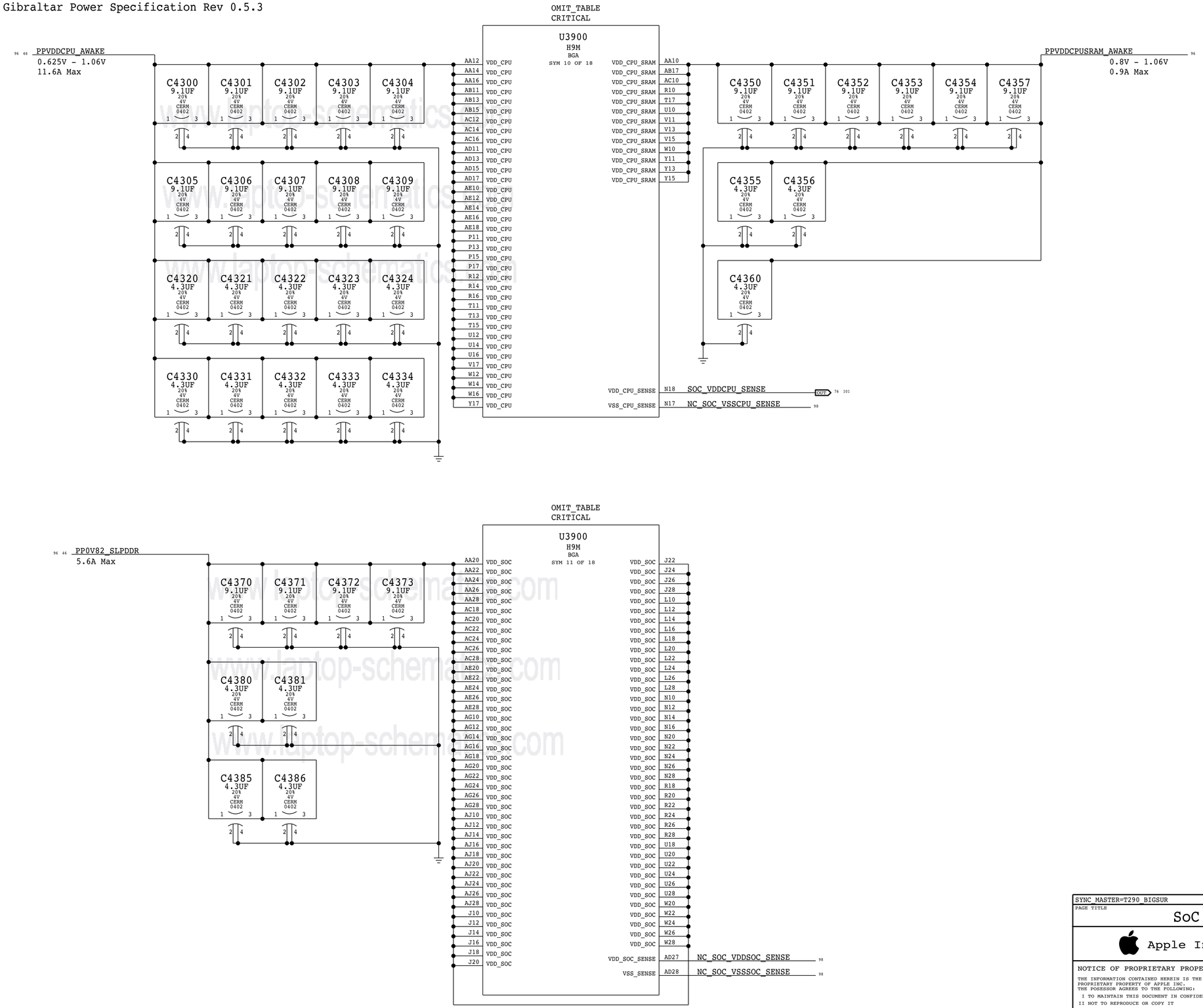
Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



BOM_COST_GROUP=SOC

SYNC_MASTER=T290_BIGSUR SYNC_DATE=03/29/2017

PAGE TITLE
SoC Power 1

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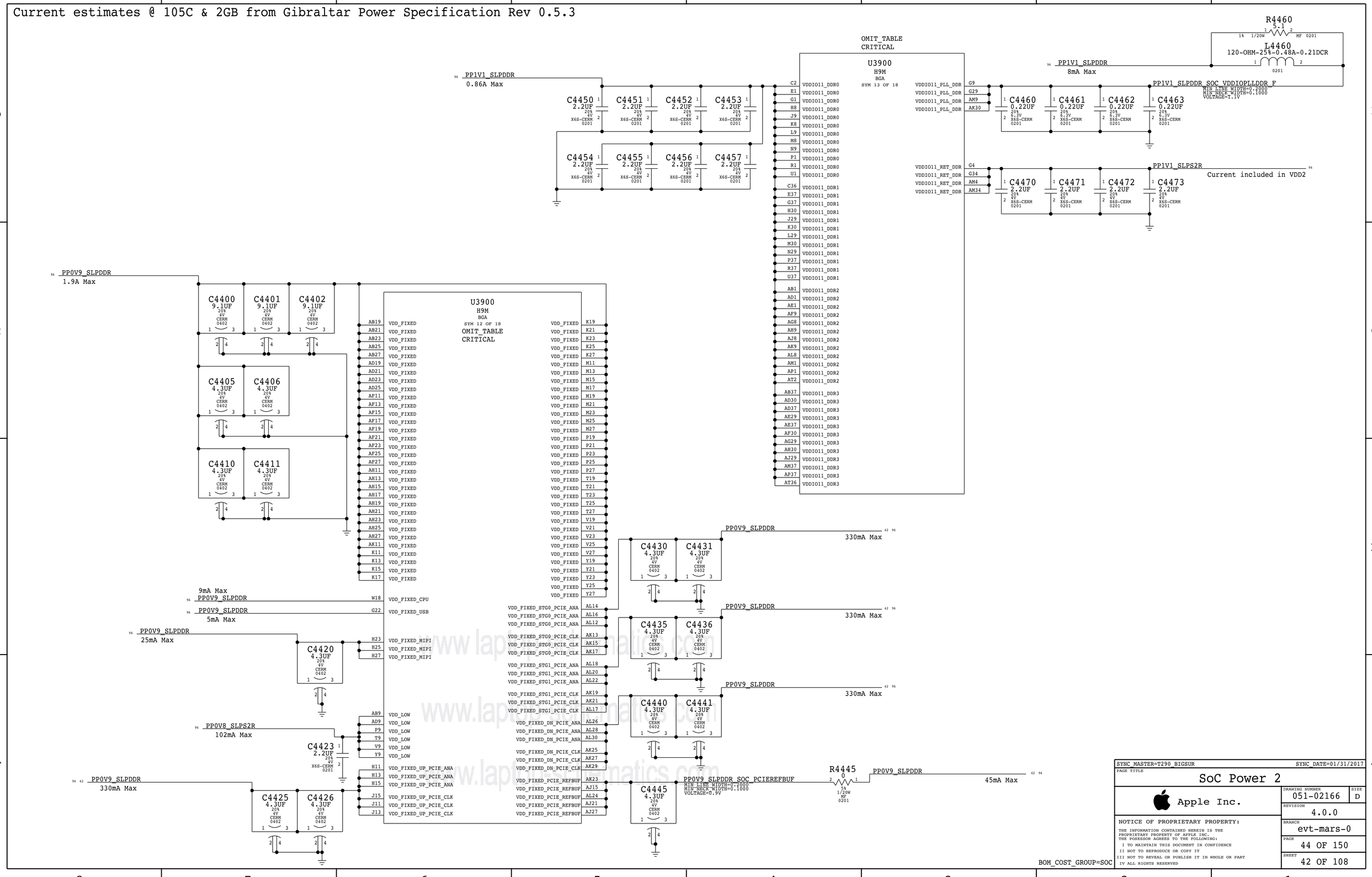
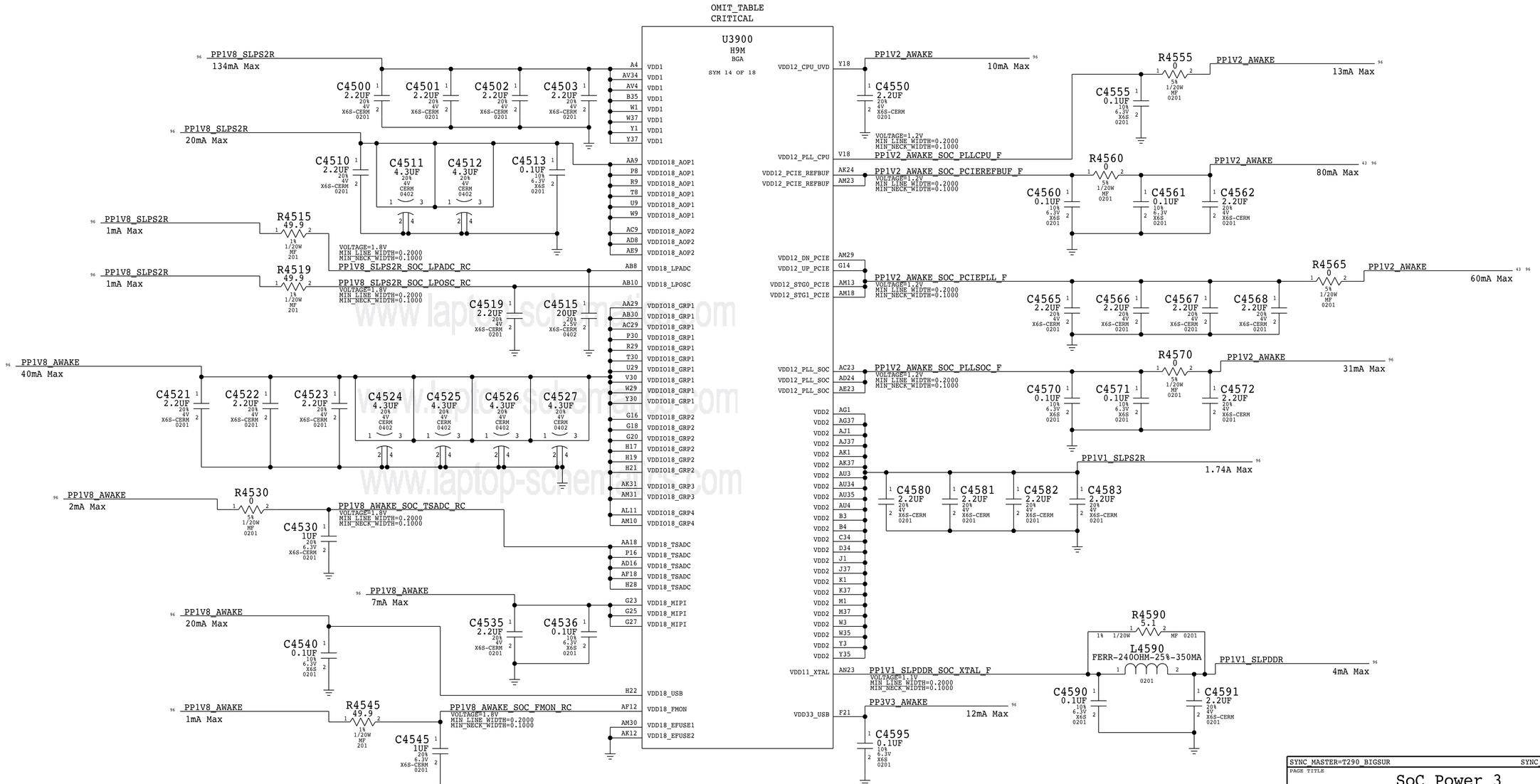


Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



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BOM_COST_GROUP=SOC

SYNC_MASTER=T290_BIGSUR SYNC_DATE=08/15/2017

PAGE TITLE

SoC Power 3

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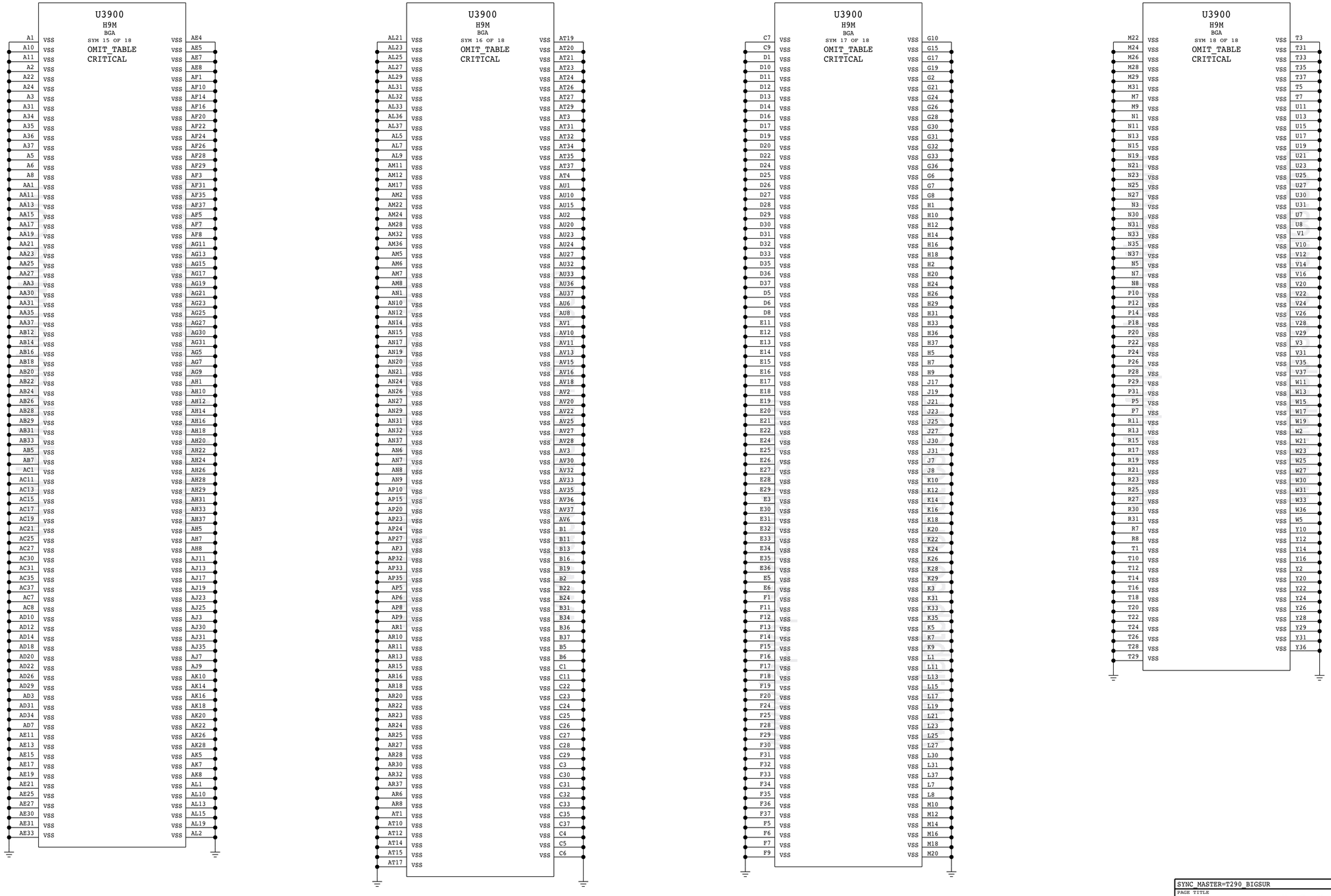

BOM_COST_GROUP=SOC

SYNC_MASTER=T290_BIGSUR SYNC_DATE=01/31/2017

PAGE TITLE

SoC Ground

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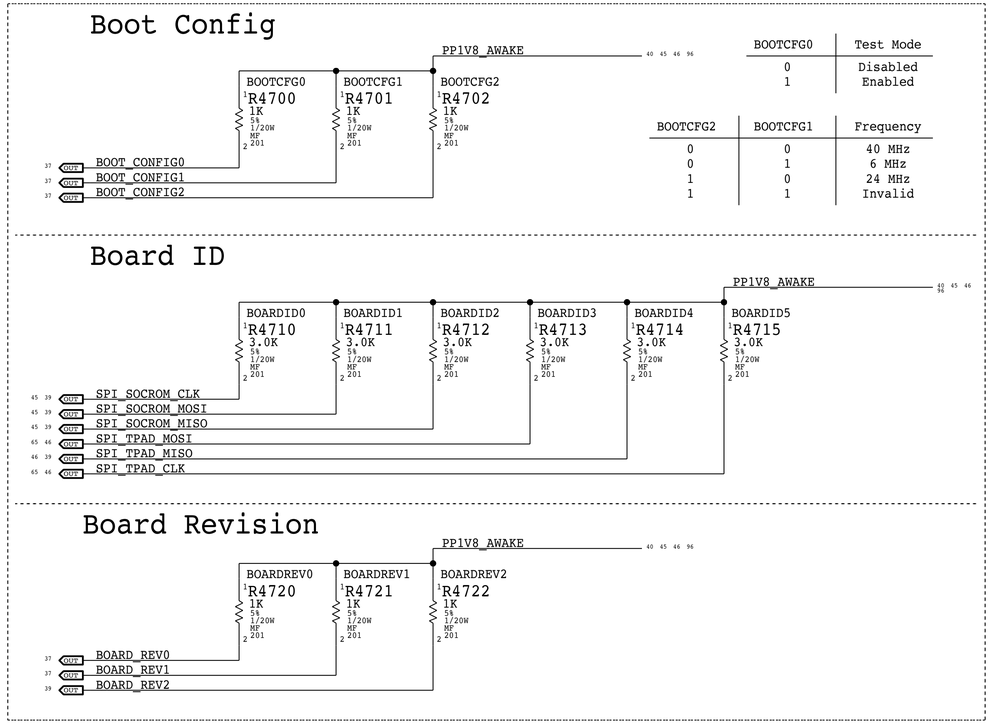
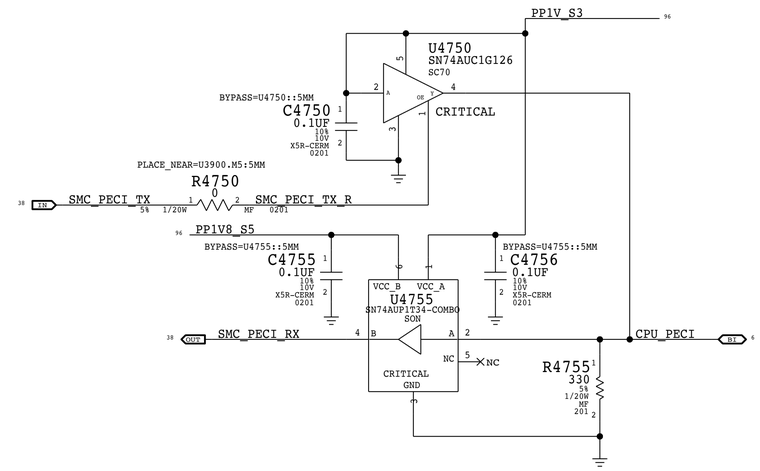


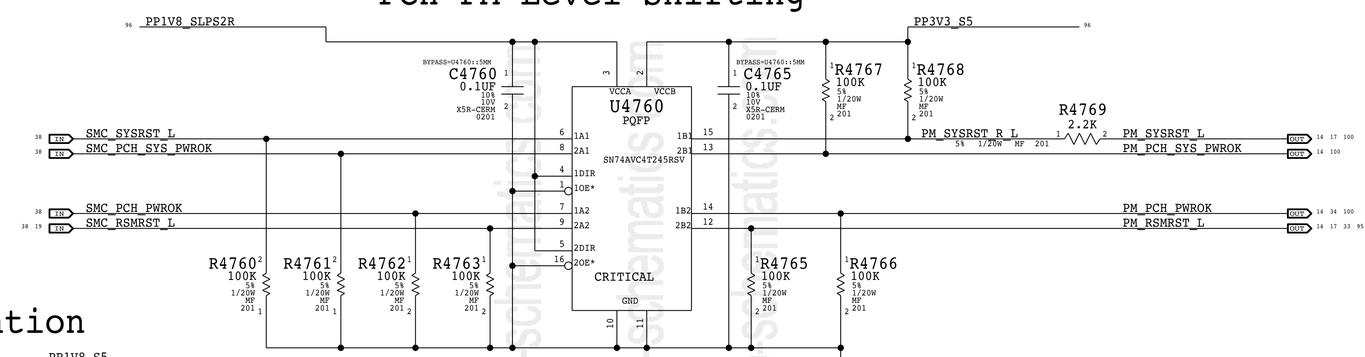
BOOTCFG0	Test Mode
0	Disabled
1	Enabled

BOOTCFG2	BOOTCFG1	Frequency
0	0	40 MHz
0	1	6 MHz
1	0	24 MHz
1	1	Invalid

PECI Level Shifting

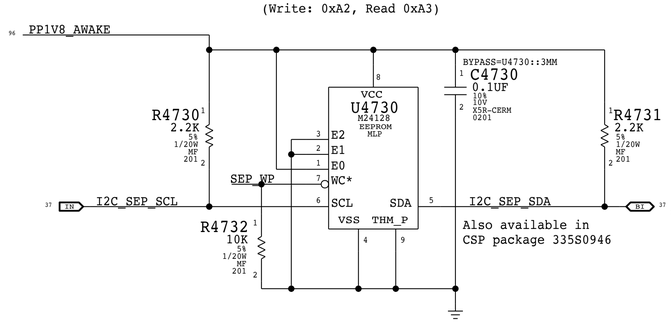


PCH PM Level Shifting

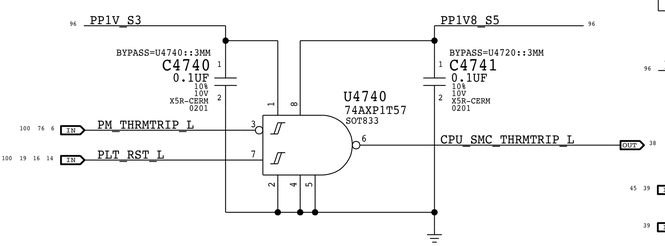


SEP EEPROM

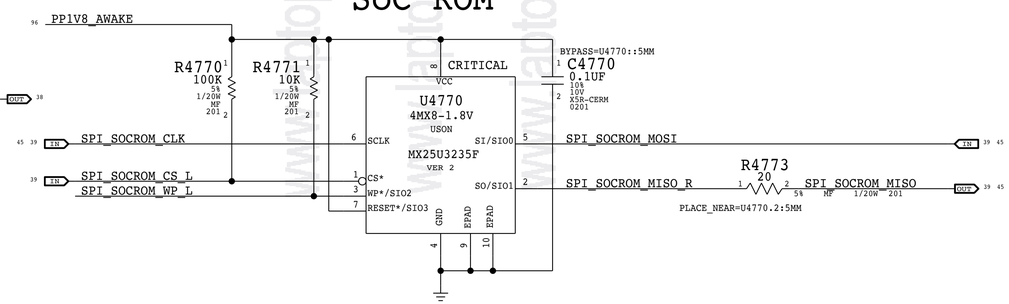
(Write: 0xA2, Read 0xA3)



THRMTRIP# Isolation

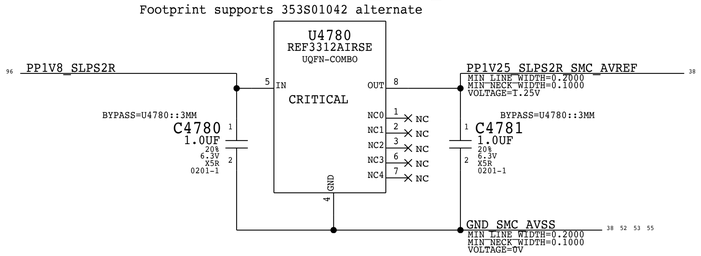


SoC ROM



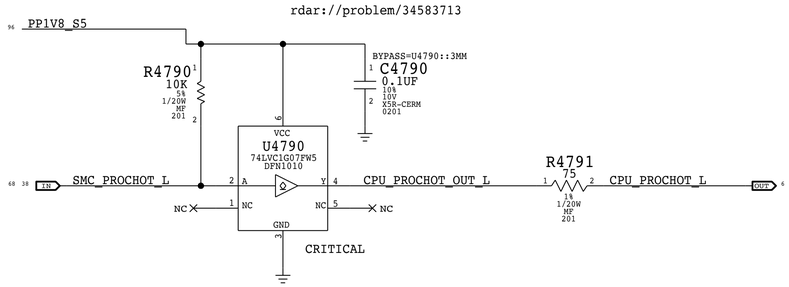
SMC AVREF Supply

Footprint supports 353S01042 alternate



PROCHOT# Level Shifting

rdar://problem/34583713



BOM_COST_GROUP=SOC

SYNC_MASTER=J132_JIN SYNC_DATE=09/05/2017

PAGE TITLE

SoC Shared Support

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D

REVISION 4.0.0

BRANCH evt-mars-0

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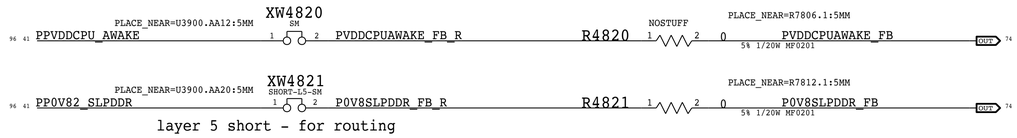
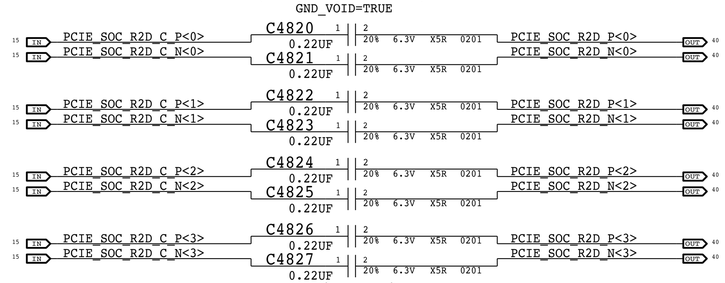
Alternate Feedback Sense



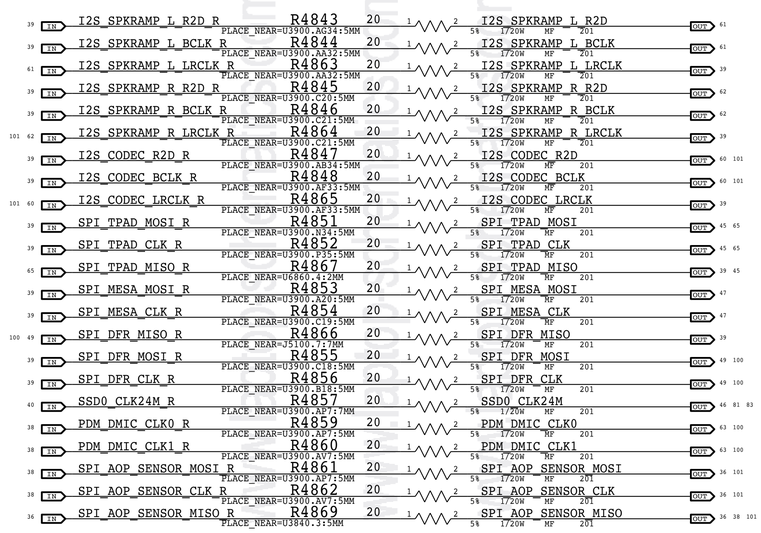
PCIe Up R2D AC Caps

(All Caps Except C4822, C4823)

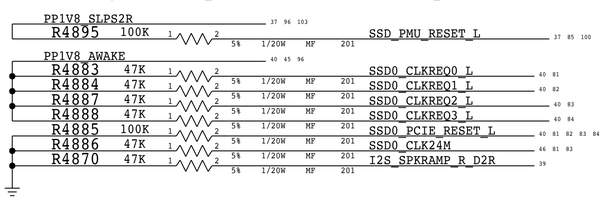
GND_VOID=TRUE



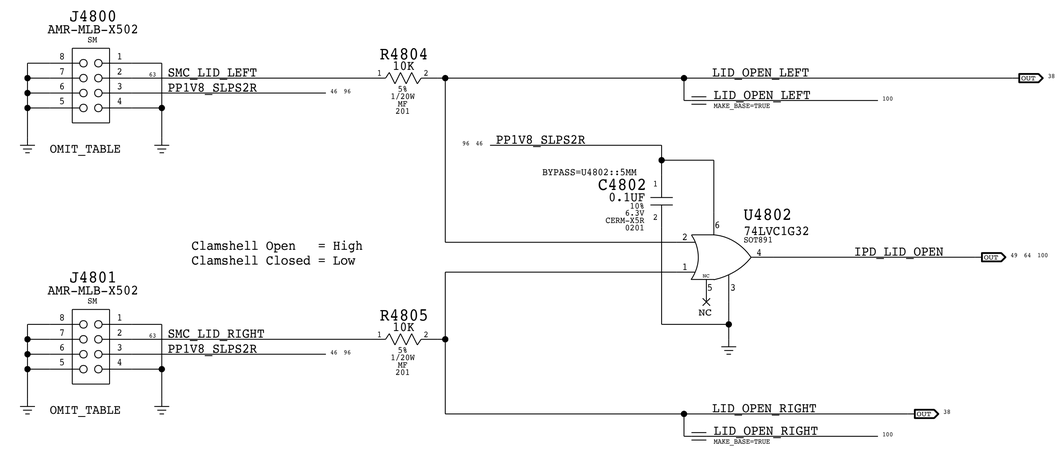
GPIO Source Termination



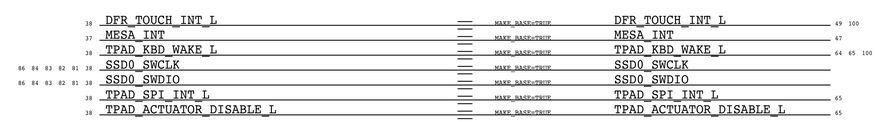
Project Specific Pull-Ups



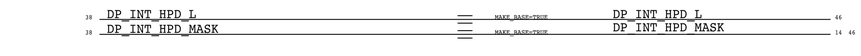
Lid Detect Sensors



SOC Overloaded GPIOs

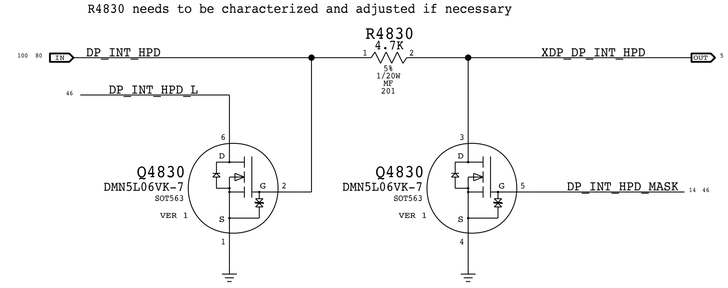


Platform-Specific GPIOs



HPD KSF Comp Circuit

R4830 needs to be characterized and adjusted if necessary



BOM GROUP	BOM OPTIONS
BOARD_REV:111	BOARDREV2,BOARDREV1,BOARDREV0
BOARD_REV:110	BOARDREV2,BOARDREV1
BOARD_REV:101	BOARDREV2,BOARDREV0
BOARD_REV:100	BOARDREV2
BOARD_REV:011	BOARDREV1,BOARDREV0

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARDID2,BOARDID3

BOM_COST_GROUP=SOC

SYNC_MASTER=J132_JACK SYNC_DATE=11/03/2017

PAGE TITLE

SoC Project Support

Apple Inc.

DRAWING NUMBER	051-02166
SIZE	D
REVISION	4.0.0
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ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

ESD Filters

R4912
47 39 OUT SPI_MESA_MISO — 0 (5% 1/20W MF 0201) — SPI_MESA_MISO_CONN 47 100
C4952 56PF 5% 25V NPO-C0G 0201

R4953
46 OUT MESA_INT — 680 (5% 1/20W MF 201) — MESA_INT_CONN 47 100
C4953 100PF 5% 25V C0G 0201

R4954
47 MESA_BOOST_EN — 680 (5% 1/20W MF 201) — MESA_BOOST_EN_CONN 47 100
C4954 100PF 5% 25V C0G 0201

T151 FLEX CONNECTOR

PLUG (516S00115) - X434/ X435 Jumper
RECEPTACLE (516S00203) - MLB

PP3V0_MESA_FILT_CONN 100 47

J4900
505066-1220
F-ST-SM

100 47	SPI_MESA_MISO_CONN	PP1V8_MESA_FILT_CONN	47 100
100 47	MESA_INT_CONN		
100 47	MESA_BOOST_EN_CONN	SPI_MESA_MOSI_CONN	47 100
NC		PMU_ONOFF_R_L_CONN	47 100
NC		SPI_MESA_CLK_CONN	47 100
		PP16V0_MESA_FILT_CONN	47 100

100 ESD_GND — P2MM SM — PP4900
MIN_LINE_WIDTH=0.0900 — P2MM SM — PP4901

ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

ESD Filters

R4950
100 47 SPI_MESA_MOSI_CONN — 0 (5% 1/20W MF 0201) — SPI_MESA_MOSI IN 46
C4950 56PF 5% 25V NPO-C0G 0201

R4951
100 47 SPI_MESA_CLK_CONN — 56 (5% 1/20W MF 201) — SPI_MESA_CLK IN 46
C4951 56PF 5% 25V NPO-C0G 0201

R4911
100 47 PMU_ONOFF_R_L_CONN — 0 (5% 1/20W MF 0201) — PMU_ONOFF_L OUT 66 76 103
C4955 100PF 5% 25V C0G 0201

Output Voltage	16.0V +/- 2%
Iout (max avg)	6mA
OCP (min)	13 mA
Active Discharge	15 mA sink
Max Output Cap	0.5uF @ 16V

Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

MOJAVE 16V BOOST

PLACE_NEAR=U4900:5MM
L4901
1.0UH-0.4A-0.6360HM
0402

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
DIDT=TRUE

PP3V3_G3H_MESA_SW

97 47 PP3V3_G3H_RTC_MESA

BYPASS=U4900.A2::3MM

C4910
10UF
20%
6.3V
CERM-X5R
0402-9

47 MESA_BOOST_EN

U4900
LM3638
BGA

B1	SW	
A2	VIN	
B2	EN_M	
A3	EN_S	
C2	LDOIN	
C3	VOUT	
C1	PMID	
A1	PGND	
B3	AGND	

Load Cap:6.6uF nom
EDP:13.75mA

C4924 2.2UF 20% 25V X5R 0402-3
C4925 2.2UF 20% 25V X5R 0402-3
C4926 56PF 5% 25V NPO-C0G 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=16V
PP16V0_MESA

BYPASS=U4900.C3::3MM
BYPASS=U4900.C3::4MM
BYPASS=U4900.C3::5MM

EMC Filter

FL4900
80-OHM-25%-500MA
0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=16V
PP16V0_MESA_FILT_CONN 47 100

C4927 100PF 5% 25V C0G 0201

VOLTAGE=17V
PP17V0_MOJAVE_LDOIN

C4923 2.2UF 20% 25V X5R 0402-3

Output Voltage	3.0V +/- 2%
Iout (max avg)	250mA
Dropout Voltage	155mV
OCP (min)	250 mA
Active Discharge	280 Ohm Typ

3.0V MESA

U4910
NCP160AMX300
XDFN-COMBO-THICKSTNCL

97 47 PP3V3_G3H_RTC_MESA — IN
C4911 1UF 10% 10V X5R-CERM 0402
BYPASS=U4910.4::3MM

47 PP1V8_MESA — EN
GND EPAD

OUT — MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.0V
Load Cap:14.3uF nom
EDP:100mA
PP3V0_MESA

BYPASS=U4910.1::3MM
C4916 1UF 10% 10V X5R-CERM 0402

EMC Filter

C4920 2.2UF 20% 6.3V X5R-CERM 0201
C4921 2.2UF 20% 6.3V X5R-CERM 0201
C4922 2.2UF 20% 6.3V X5R-CERM 0201

FL4910
80-OHM-25%-500MA
0201

C4928 0.1UF 10% 10V X5R-CERM 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.0V
PP3V0_MESA_FILT_CONN 47 100

C4929 100PF 5% 25V C0G 0201

Output Voltage	1.825V +/- 2%
Iout (max avg)	250mA
Dropout Voltage	50mV Typ @ 100mA
OCP (min)	250 mA
Active Discharge	230 Ohm Typ
Max Output Cap	10uF

1.8V MESA

U4920
LP5907SNX-1.825
X2SON-COMBO-THICKSTNCL

97 47 PP3V3_G3H_RTC_MESA — VIN
C4912 1UF 10% 10V X5R-CERM 0402
BYPASS=U4920.4::3MM

47 37 IN MESA_PWR_EN — EN
GND EPAD

VOUT — MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.825V
Load Cap:3.4uF nom
EDP:0.5mA
47 PP1V8_MESA

BYPASS=U4920.1::3MM
C4914 1UF 10% 10V X5R-CERM 0402

EMC Filter

C4918 2.2UF 20% 6.3V X5R-CERM 0201

FL4920
80-OHM-25%-500MA
0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.825V
PP1V8_MESA_FILT_CONN 47 100

C4917 100PF 5% 25V C0G 0201

PP1V8_G3S 97
R4922 100K (5% 1/20W MF 201) MESA_PWR_EN 37 47

PP1V8_MESA 47
R4924 100K (5% 1/20W MF 201) SPI_MESA_MISO 39 47
R4923 100K (5% 1/20W MF 201) MESA_BOOST_EN 47

BOM_COST_GROUP=T151

PAGE TITLE	T151
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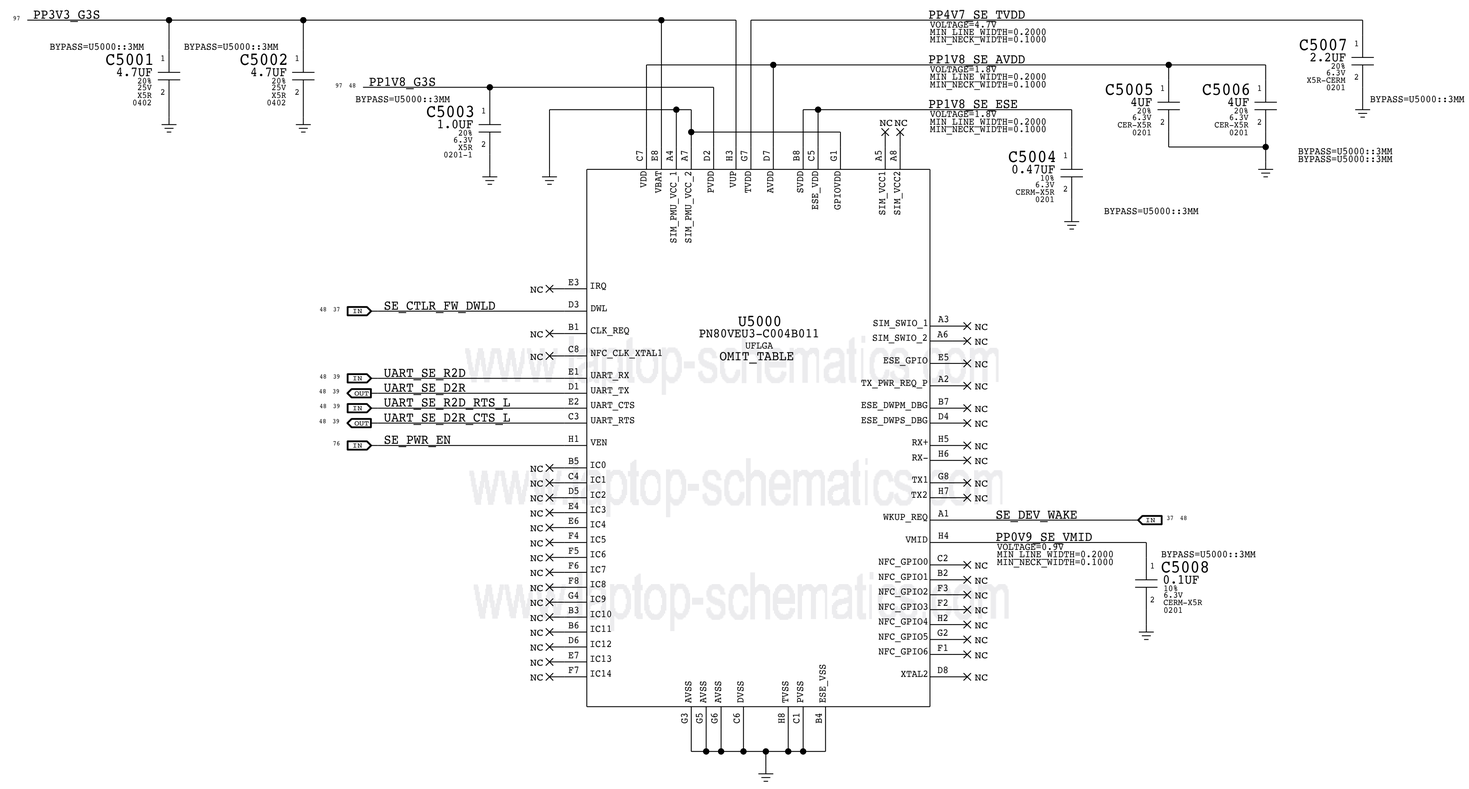

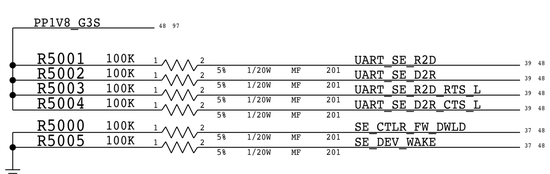

BOM_COST_GROUP=SOC

SYNC_MASTER=J132_GREG SYNC_DATE=05/16/2017

PAGE TITLE

Secure Element

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REVISION 4.0.0

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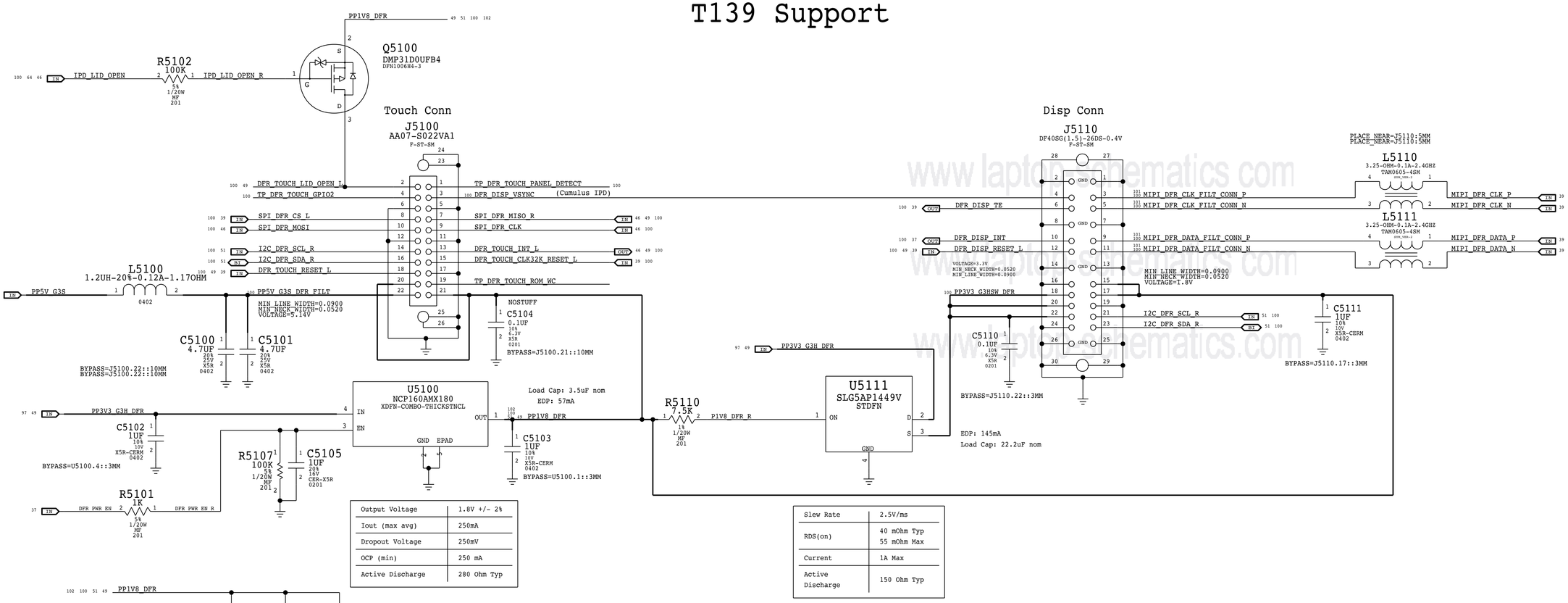
T139 Support



Output Voltage	1.8V +/- 2%
Iout (max avg)	250mA
Dropout Voltage	250mV
OCP (min)	250 mA
Active Discharge	280 Ohm Typ

Slew Rate	2.5V/ms
RDS(on)	40 mOhm Typ 55 mOhm Max
Current	1A Max
Active Discharge	150 Ohm Typ

BOM_COST_GROUP=T139

PAGE TITLE: T139 Support

Apple Inc.

DRAWING NUMBER: 051-02166 SIZE: D

REVISION: 4.0.0

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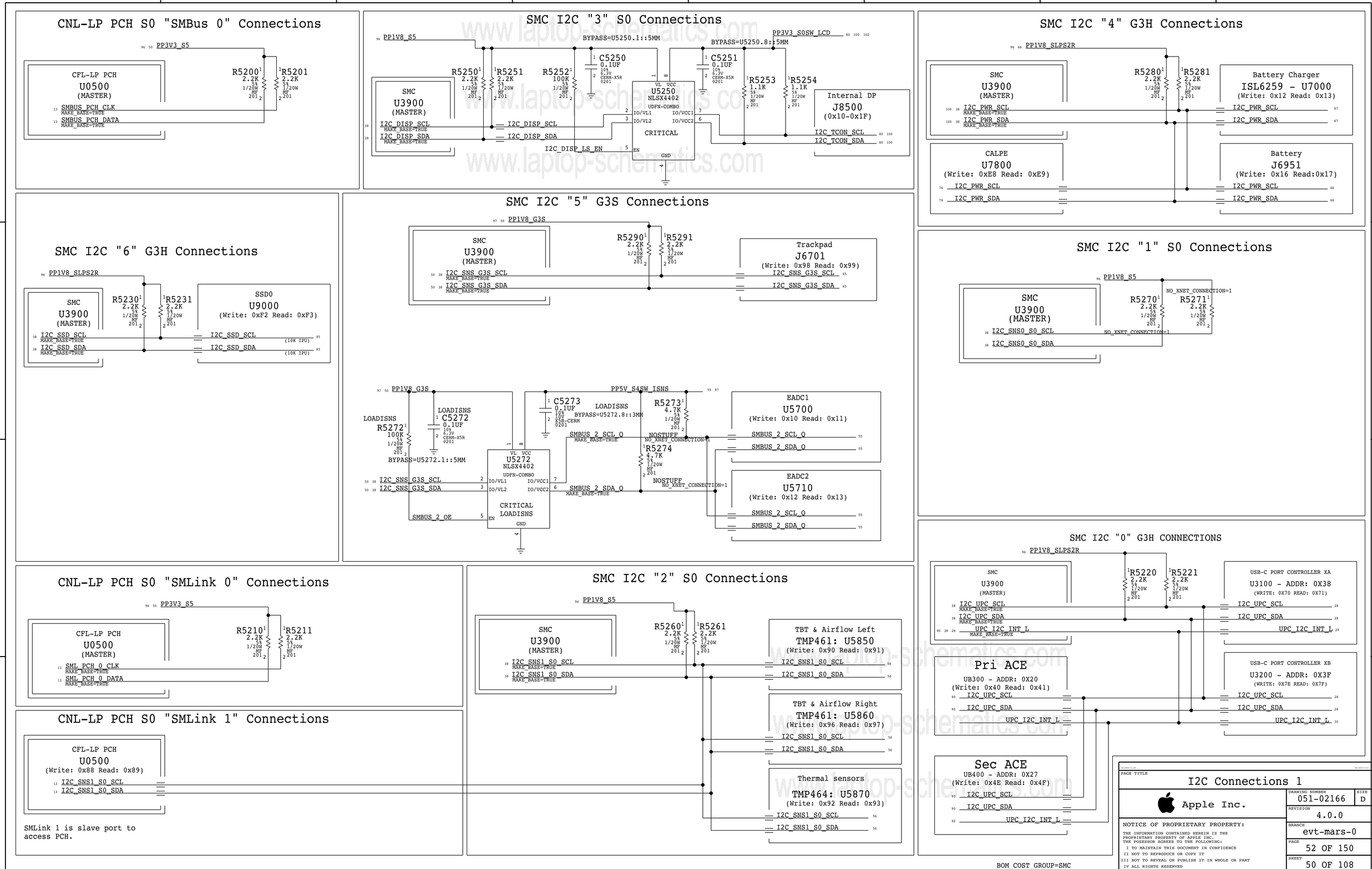
CNL-LP PCH S0 "SMBus 0" Connections
PP3V3_S5
CFL-LP PCH
U0500
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
R5200 2.2K
R5201 2.2K
SMC I2C "3" S0 Connections
PP1V8_S5
BYPASS=U5250.1::5MM
PP3V3_S0SW_LCD
BYPASS=U5250.8::5MM
SMC
U3900
(MASTER)
I2C_DISP_SCL
I2C_DISP_SDA
I2C_DISP_LS_EN
R5250 2.2K
R5251 2.2K
R5252 100K
C5250 0.1UF
C5251 0.1UF
U5250
NLSX4402
UDFN-COMBO
CRITICAL
R5253 1.1K
R5254 1.1K
Internal DP
J8500
(0x10-0x1F)
I2C_TCON_SCL
I2C_TCON_SDA
SMC I2C "4" G3H Connections
PP1V8_SLPS2R
SMC
U3900
(MASTER)
I2C_PWR_SCL
I2C_PWR_SDA
R5280 2.2K
R5281 2.2K
Battery Charger
ISL6259 - U7000
(Write: 0x12 Read: 0x13)
CALPE
U7800
(Write: 0xE8 Read: 0xE9)
Battery
J6951
(Write: 0x16 Read:0x17)
SMC I2C "6" G3H Connections
PP1V8_SLPS2R
SMC
U3900
(MASTER)
I2C_SSD_SCL
I2C_SSD_SDA
R5230 2.2K
R5231 2.2K
SSD0
U9000
(Write: 0xF2 Read: 0xF3)
(10K IPU)
SMC I2C "5" G3S Connections
PP1V8_G3S
SMC
U3900
(MASTER)
I2C_SNS_G3S_SCL
I2C_SNS_G3S_SDA
R5290 2.2K
R5291 2.2K
Trackpad
J6701
(Write: 0x98 Read: 0x99)
I2C_SNS_G3S_SCL
I2C_SNS_G3S_SDA
PP1V8_G3S
LOADISNS
R5272 100K
C5272 0.1UF
BYPASS=U5272.1::5MM
U5272
NLSX4402
UDFN-COMBO
CRITICAL
LOADISNS
SMBUS_2_OE
C5273 0.1UF
BYPASS=U5272.8::3MM
PP5V_S4SW_ISNS
R5273 4.7K
R5274 4.7K
NOSTUFF
NO_XNET_CONNECTION=1
SMBUS_2_SCL_O
SMBUS_2_SDA_O
EADC1
U5700
(Write: 0x10 Read: 0x11)
EADC2
U5710
(Write: 0x12 Read: 0x13)
SMC I2C "1" S0 Connections
PP1V8_S5
SMC
U3900
(MASTER)
I2C_SNS0_S0_SCL
I2C_SNS0_S0_SDA
R5270 2.2K
R5271 2.2K
NO_XNET_CONNECTION=1
CNL-LP PCH S0 "SMLink 0" Connections
PP3V3_S5
CFL-LP PCH
U0500
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA
R5210 2.2K
R5211 2.2K
CNL-LP PCH S0 "SMLink 1" Connections
CFL-LP PCH
U0500
(Write: 0x88 Read: 0x89)
I2C_SNS1_S0_SCL
I2C_SNS1_S0_SDA
SMLink 1 is slave port to
access PCH.
SMC I2C "2" S0 Connections
PP1V8_S5
SMC
U3900
(MASTER)
I2C_SNS1_S0_SCL
I2C_SNS1_S0_SDA
R5260 2.2K
R5261 2.2K
TBT & Airflow Left
TMP461: U5850
(Write: 0x90 Read: 0x91)
TBT & Airflow Right
TMP461: U5860
(Write: 0x96 Read: 0x97)
Thermal sensors
TMP464: U5870
(Write: 0x92 Read: 0x93)
SMC I2C "0" G3H CONNECTIONS
PP1V8_SLPS2R
SMC
U3900
(MASTER)
I2C_UPC_SCL
I2C_UPC_SDA
UPC_I2C_INT_L
R5220 2.2K
R5221 2.2K
USB-C PORT CONTROLLER XA
U3100 - ADDR: 0X38
(WRITE: 0X70 READ: 0X71)
USB-C PORT CONTROLLER XB
U3200 - ADDR: 0X3F
(WRITE: 0X7E READ: 0X7F)
Pri ACE
UB300 - ADDR: 0X20
(Write: 0x40 Read: 0x41)
Sec ACE
UB400 - ADDR: 0X27
(Write: 0x4E Read: 0x4F)
BOM_COST_GROUP=SMC
PAGE TITLE
I2C Connections 1
Apple Inc.
DRAWING NUMBER 051-02166
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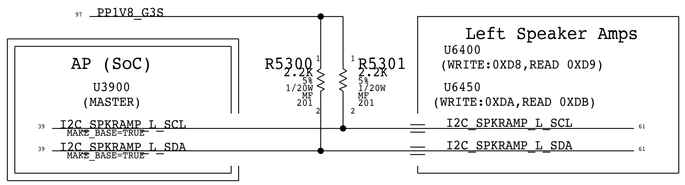
AP I2C "0" G3S Connections



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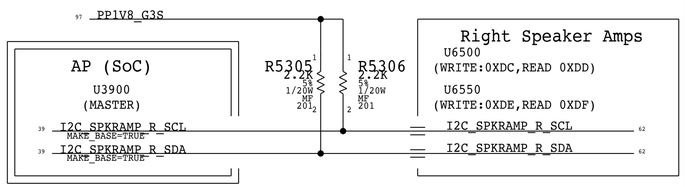
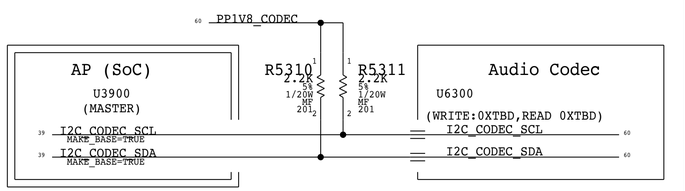


AP I2C "2" Codec Connections



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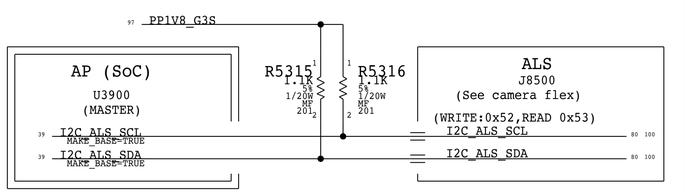
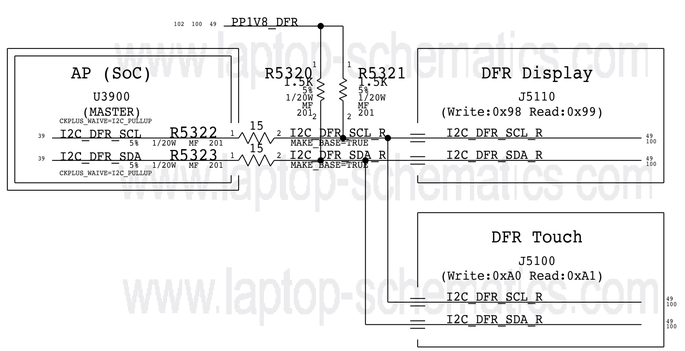
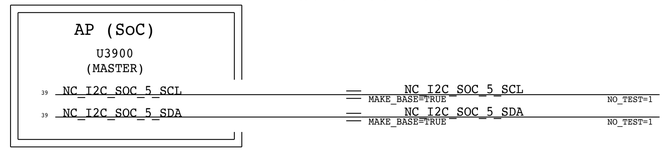


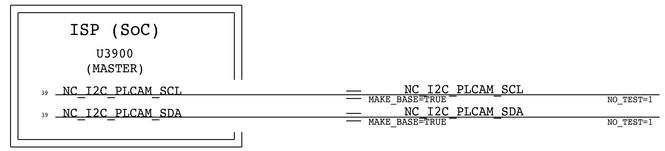
AP I2C "4" DFR Connections



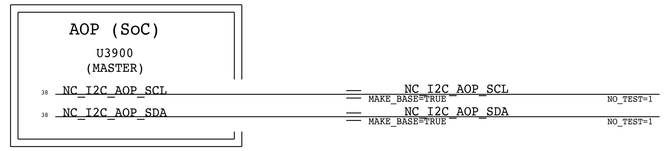
AP I2C "5" Awake Connections



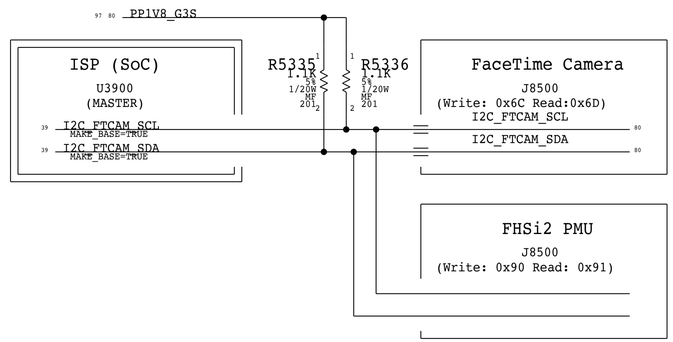
ISP I2C "1" G3S Connections



AOP I2C "0" G3S Connections



ISP I2C "0" G3S Connections



Device	SMC IF	ADDR. (8b)
ACE XA	I2C0	0X70/1
ACE XB	I2C0	0X7E/F
ACE TA	I2C0	0X40/1
ACE TB	I2C0	0X4E/F
NC.	I2C1	
Temp. Sensor Left	I2C2	0X90/1
Temp. Sensor Right	I2C2	0X96/7
Plateform Thermal Sensor	I2C2	0X92/3
PCH	I2C2	0X88/9
TCON	I2C3	0X10-1F
Charger	I2C4	0X12/3
Battery	I2C4	0X16/7
Calpe	I2C4	0XE8/9
Trackpad	I2C5	0X98/9
EADC1	I2C5	0X10/1
EADC2	I2C5	0X12/3
SSD	I2C6	0XF2/3
SoC IF		
Left Spkr Amp.(U6400)	I2C0	0XD8/9
Left Spkr Amp.(U6450)	I2C0	0XDA/B
Right Spkr Amp.(U6500)	I2C1	0XDC/D
Right Spkr Amp.(U6550)	I2C1	0XDE/F
Audio Codec	I2C2	0X90/1
ALS	I2C3	0X52/3
DFR Display	I2C4	0X98/9
DFR Touch	I2C4	0XA0/1
NC.	I2C5	
Spkr ID1	I2C6	
Spkr ID0	I2C6	
SIP IF		
FT Camera	I2C0	0X6C/D
FHSi2	I2C0	0X90/1
NC.	I2C1	
AOP IF		
NC.	I2C0	

BOM_COST_GROUP=SMC

PAGE TITLE
I2C Connections 2

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DRAWING NUMBER 051-02166
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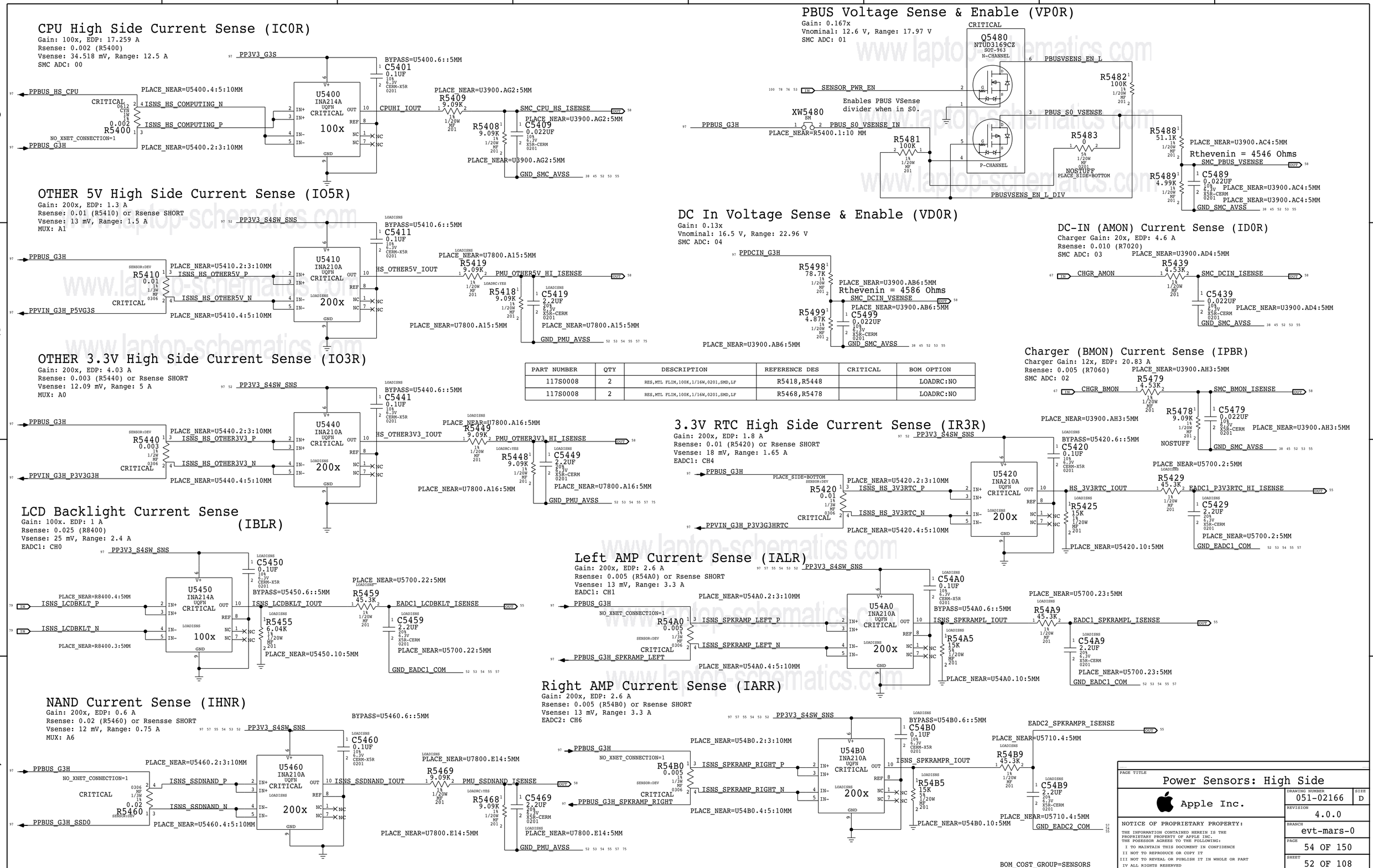
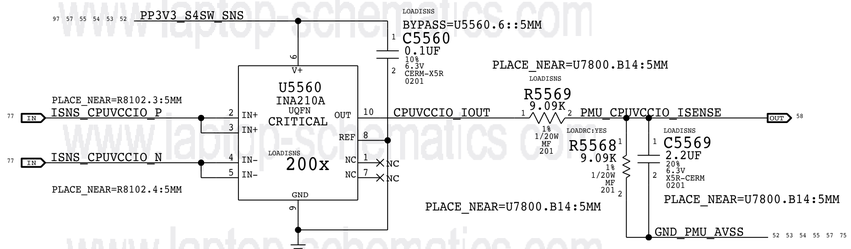


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5418,R5448		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5468,R5478		LOADRC:NO

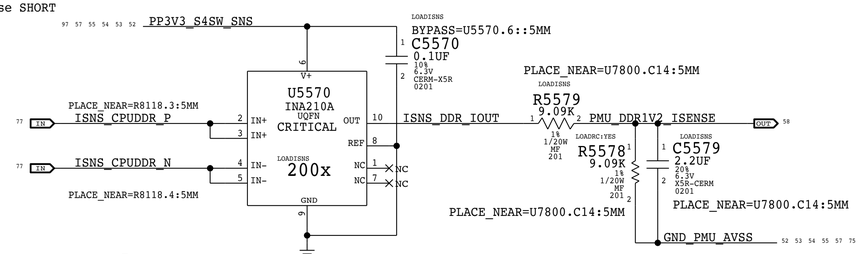
CPU VCCIO Current Sense (IC1C)

Gain: 200x, EDP: 3.6 A
Rsense: 0.003 (R8102) or Rsense SHORT
Vsense: 10.8 mV, Range: 5 A
MUX: A3



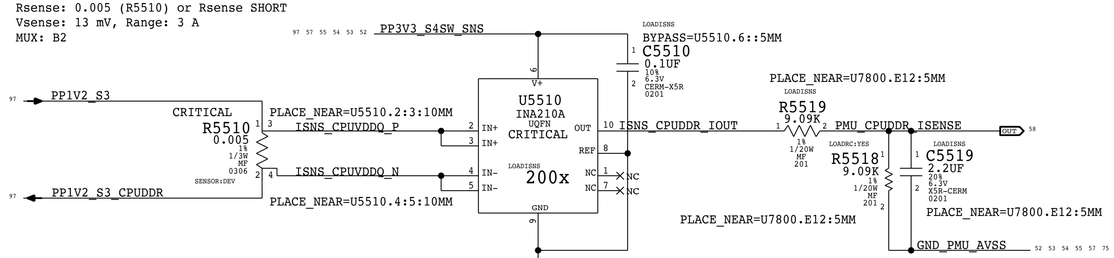
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 200x, EDP: 6.9 A
Rsense: 0.002 (R8118) or Rsense SHORT
Vsense: 13.8 mV, Range: 7.5 A
MUX: A4



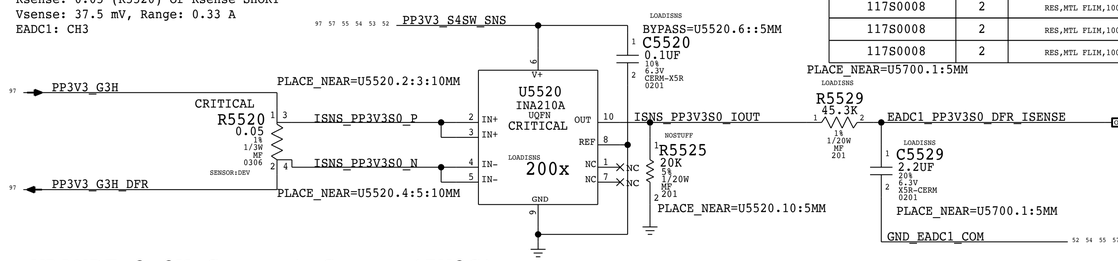
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2.6 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 13 mV, Range: 3 A
MUX: B2



DFR Current Sense (IF3C)

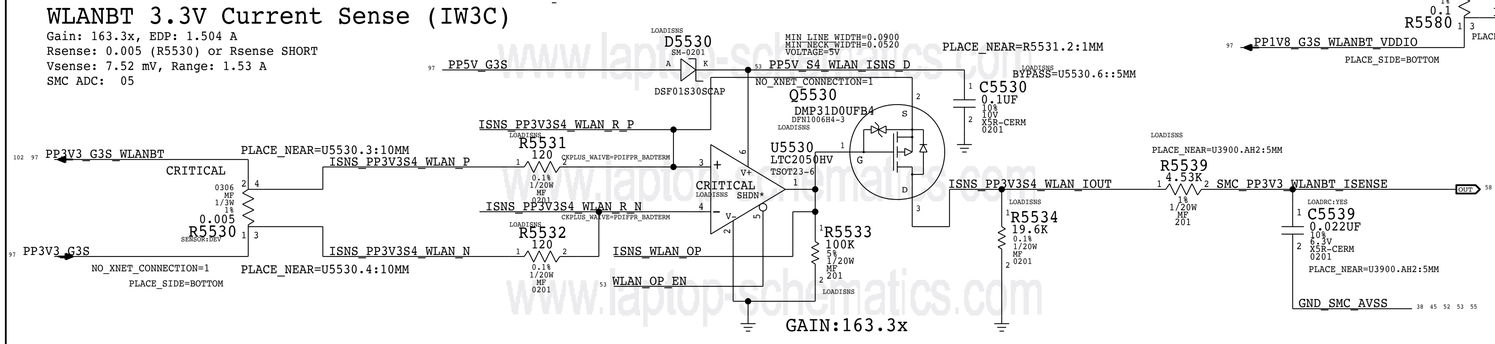
Gain: 200x, EDP: 0.75 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 37.5 mV, Range: 0.33 A
EADC1: CH3



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5568,R5518		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R554A,R5578		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5539,R5588		LOADRC:NO

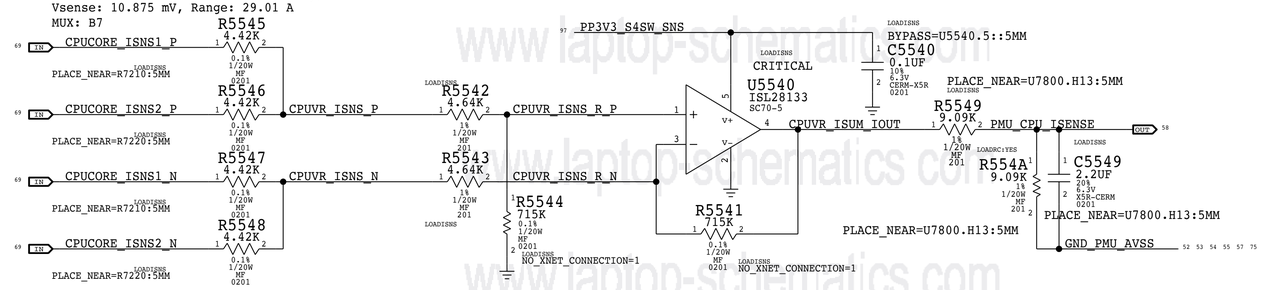
WLANBT 3.3V Current Sense (IW3C)

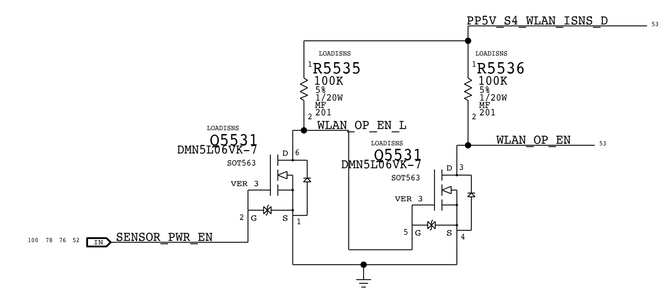
Gain: 163.3x, EDP: 1.504 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 7.52 mV, Range: 1.53 A
SMC ADC: 05



CPU Fixed Current Sense (ICAC)

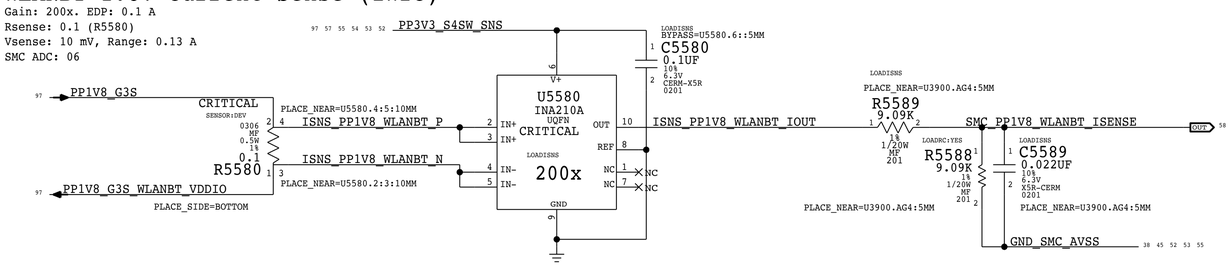
Gain: 275.74x, EDP: 29 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 10.875 mV, Range: 29.01 A
MUX: B7





WLANBT 1.8V Current Sense (IW2C)

Gain: 200x. EDP: 0.1 A
Rsense: 0.1 (R5580)
Vsense: 10 mV, Range: 0.13 A
SMC ADC: 06



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Load Side

Apple Inc.

DRAWING NUMBER: 051-02166 SIZE: D
REVISION: 4.0.0
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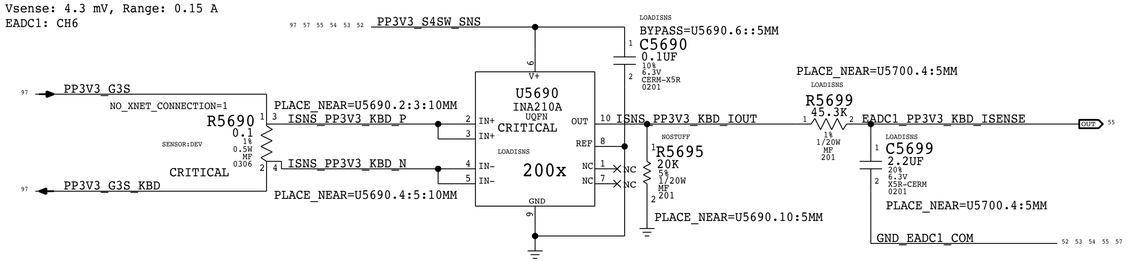
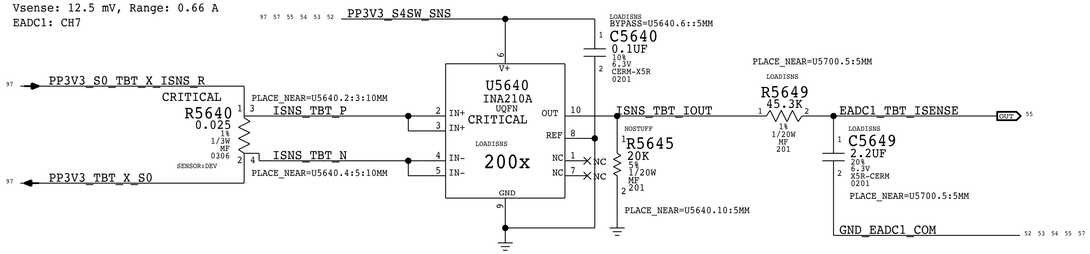
Keyboard 3V Current Sense (IK3C)

Gain: 200x, EDP: 0.043 A
Rsense: 0.1 (R5690) or Rsense SHORT
Vsense: 4.3 mV, Range: 0.15 A
EADC1: CH6



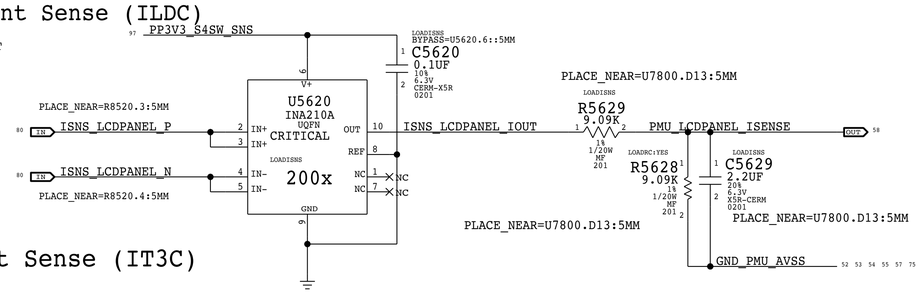
Thunderbolt TBT Current Left (IULC)

Gain: 200x. EDP: 0.8 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.66 A
EADC1: CH7



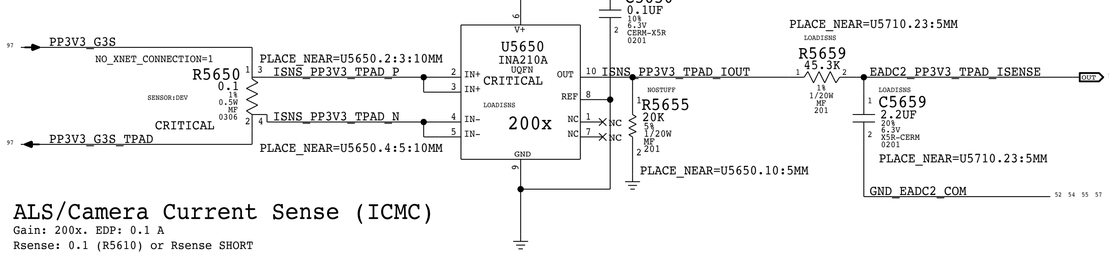
LCD Panel 3V Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.65 A
EADC2: CH0



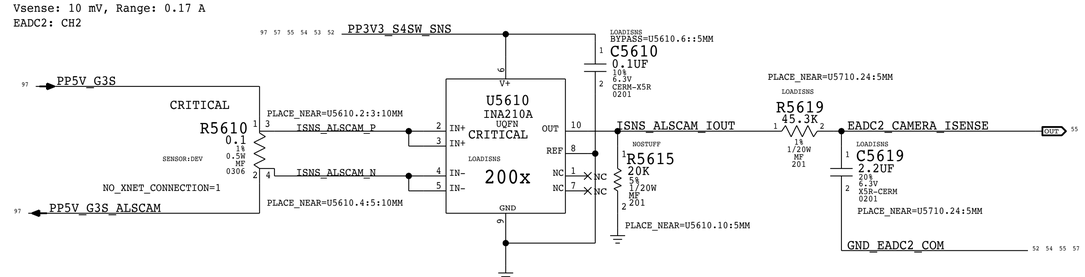
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.05 A
Rsense: 0.1 (R5650) or Rsense SHORT
Vsense: 5 mV, Range: 0.17 A
EADC2: CH1



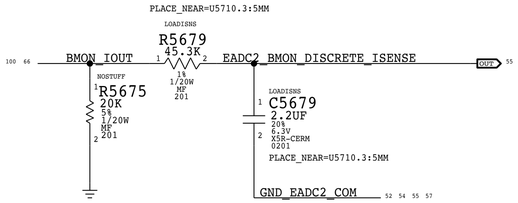
ALS/Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.1 A
Rsense: 0.1 (R5610) or Rsense SHORT
Vsense: 10 mV, Range: 0.17 A
EADC2: CH2



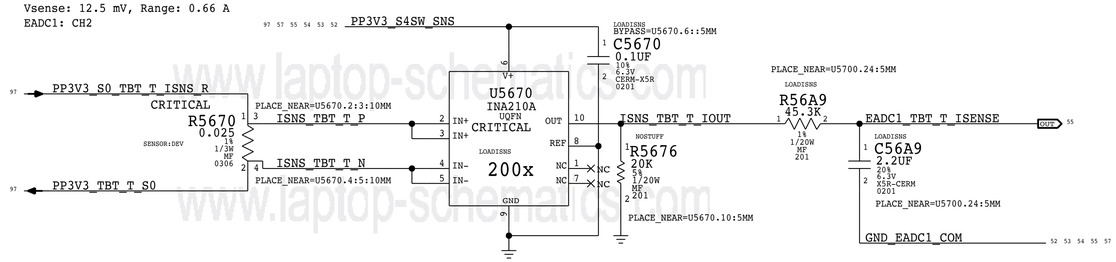
Battery Discrete Current Sense (IB0L)

Gain: 2940x. EDP: 8 A
Rsense: 0.003 (R501//R502)
Vsense: 24 mV, Range: 0.28 A
EADC2: CH5



Thunderbolt TBT Current Right (IURC)

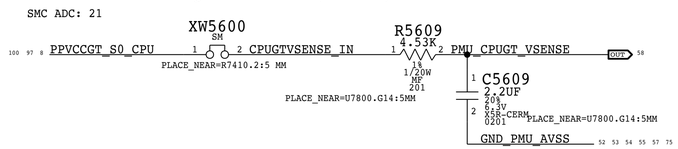
Gain: 200x. EDP: 0.8 A
Rsense: 0.025 (R5670) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.66 A
EADC1: CH2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5698,R5628		LOADRC:NO

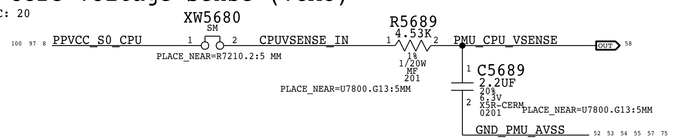
CPU GT Voltage Sense (VCGC)

SMC ADC: 21



CPU Core Voltage Sense (VCAC)

SMC ADC: 20



BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors: Extended

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D
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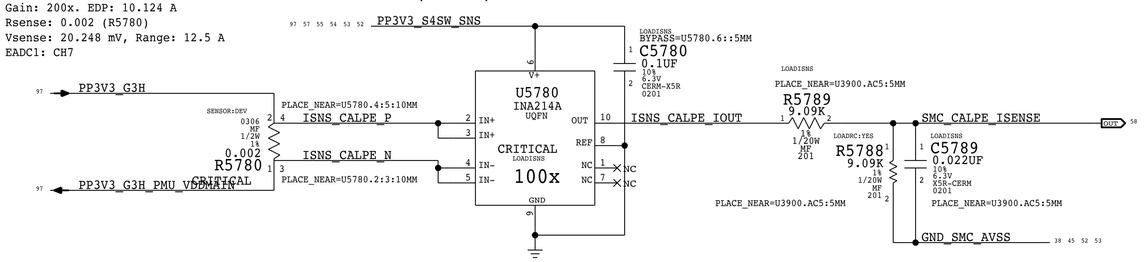
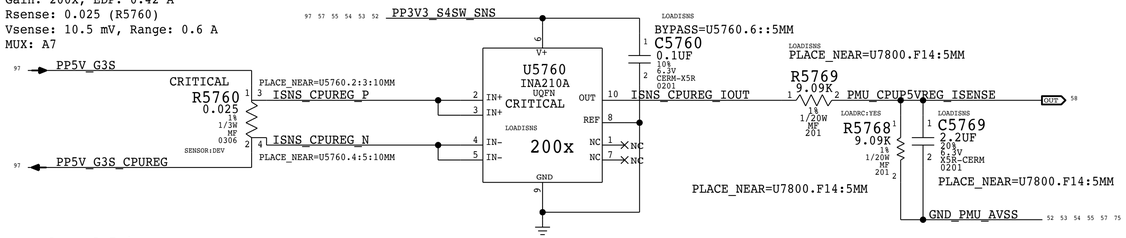
CALPE 3.3V INPUT Current Left (IP3C)

Gain: 200x. EDP: 10.124 A
Rsense: 0.002 (R5780)
Vsense: 20.248 mV, Range: 12.5 A
EADC1: CH7



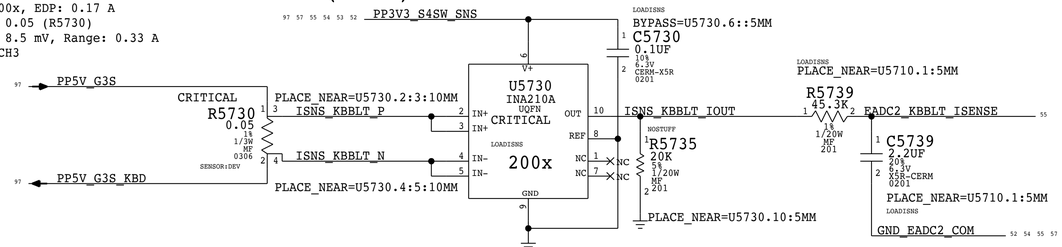
CPU REG.5V Current Sense (IC5C)

Gain: 200x, EDP: 0.42 A
Rsense: 0.025 (R5760)
Vsense: 10.5 mV, Range: 0.6 A
MUX: A7



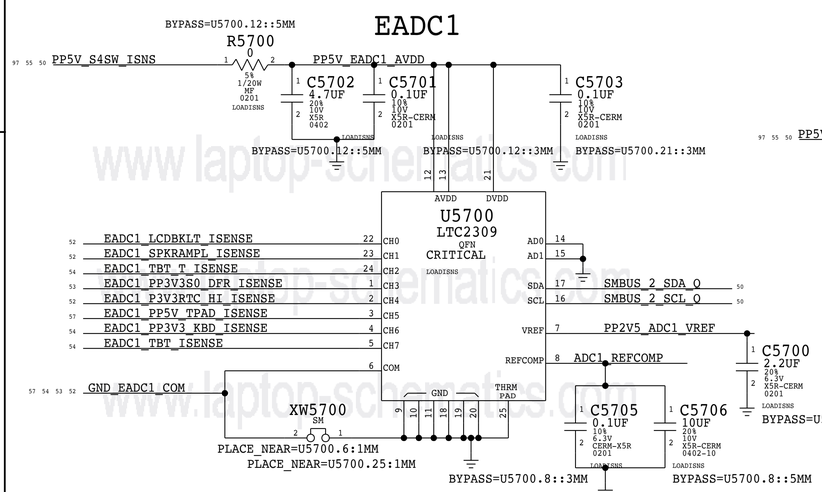
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 0.17 A
Rsense: 0.05 (R5730)
Vsense: 8.5 mV, Range: 0.33 A
EADC2: CH3

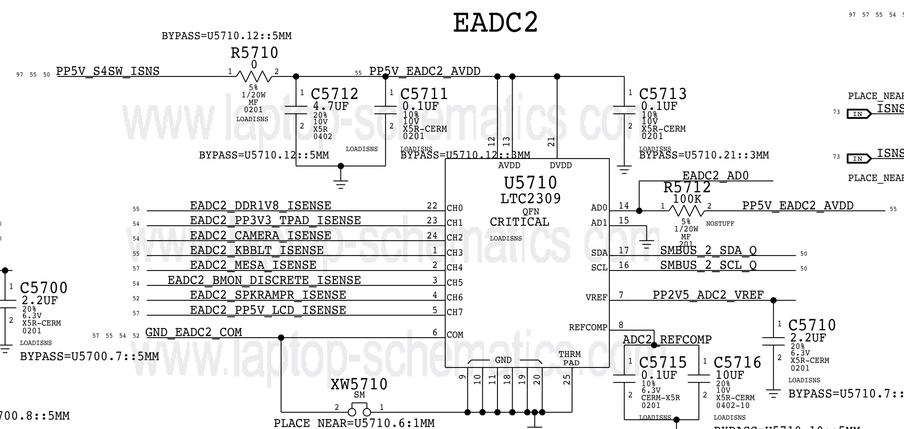


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5768,R5777		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R574A,R5788		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5798		LOADRC:NO

EADC1

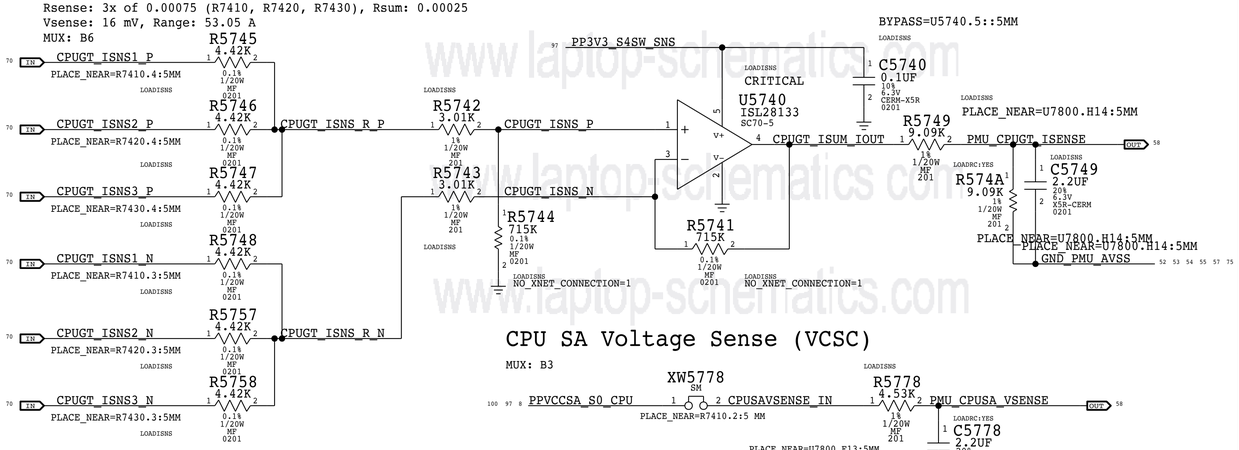


EADC2



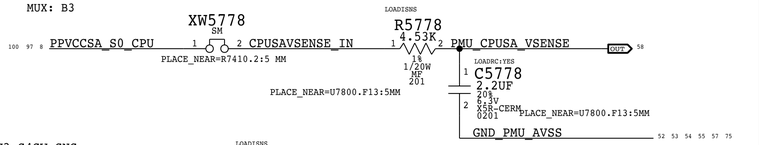
CPU GT+GTX Current Sense (ICGC)

Gain: 188.49x, EDP: 64 A
Rsense: 3x of 0.00075 (R7410, R7420, R7430), Rsum: 0.00025
Vsense: 16 mV, Range: 53.05 A
MUX: B6



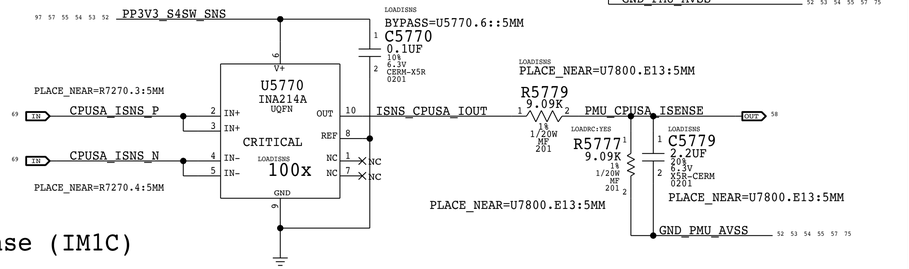
CPU SA Voltage Sense (VCSC)

MUX: B3



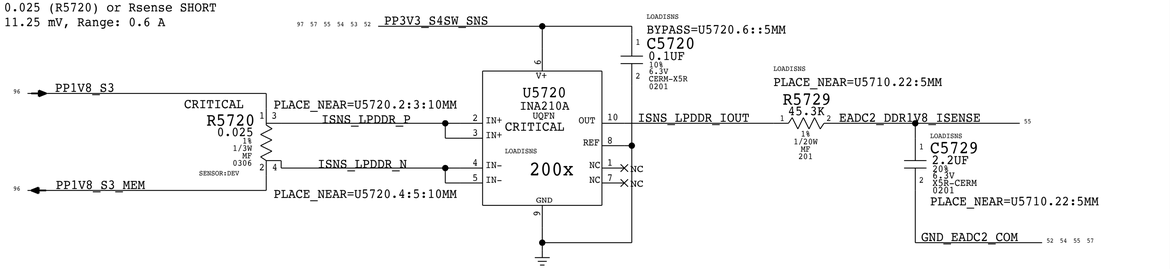
CPU SA Current Sense (ICSC)

Gain: 100x, EDP: 9.5 A
Rsense: 0.002 (R7270)
Vsense: 19 mV, Range: 15 A
MUX: B1



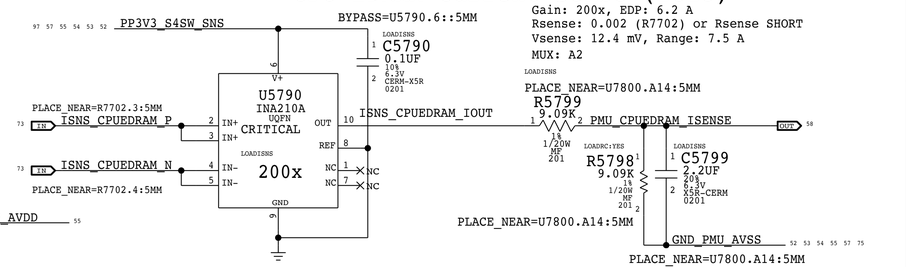
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.45 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 11.25 mV, Range: 0.6 A
MUX: B0



CPU EDRAM Current Sense (ICEC)

Gain: 200x, EDP: 6.2 A
Rsense: 0.002 (R7702) or Rsense SHORT
Vsense: 12.4 mV, Range: 7.5 A
MUX: A2



PAGE TITLE
Power Sensors: Extended 2

Apple Inc.

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BOM_COST_GROUP=SENSORS

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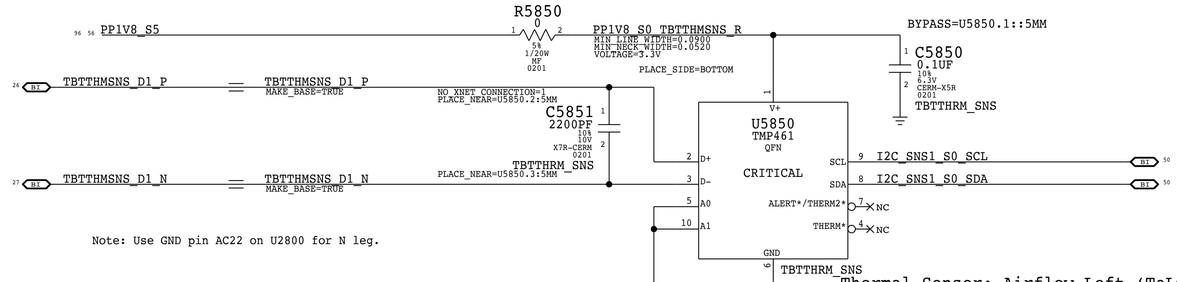
Thermal Sensor A: Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Note: Use GND pin AC22 on U2800 for N leg.

U5850 I2C Address: TMP461 is 0x90/0x91.

Thermal Sensor: Airflow Left (TaLC)

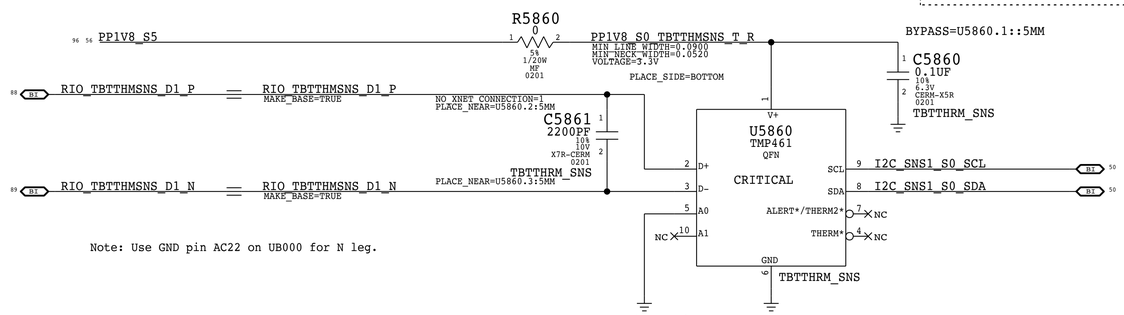
Placement Note:
Place U5860 on the BOTTOM side, at the lower corner near left fan.

Thermal Sensor C: Thunderbolt Die, Air Flow Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: TBT Die (TTRD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Note: Use GND pin AC22 on UB000 for N leg.

U5860 I2C Address: TMP461 is 0x96/0x97.

Thermal Sensor: Airflow Right (TaRC)

Placement Note:
Place U5860 on the BOTTOM side, at the lower corner near right fan.

Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.

Thermal Diode: CPU Proximity (TC0P)

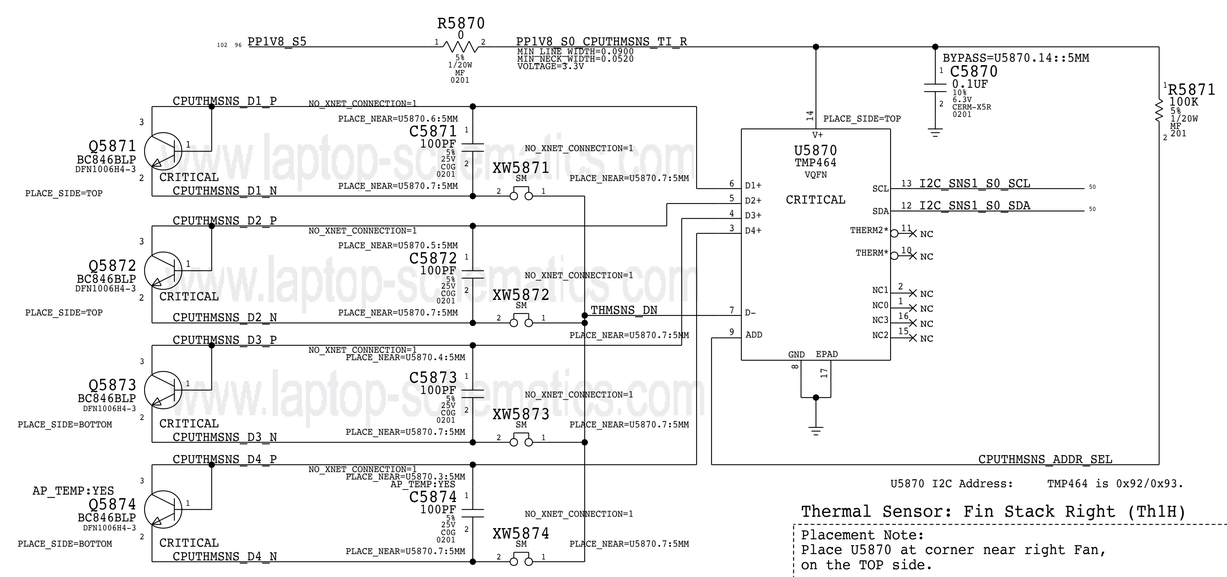
Placement Note:
Place Q5872 under the CPU, on the TOP side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5873 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

HARPOON PROXIMITY (TW0P)

Placement note:
PLACE Q5874 ON BOTTOM NEAR HARPOON



U5870 I2C Address: TMP464 is 0x92/0x93.

Thermal Sensor: Fin Stack Right (Th1H)

Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,MTL FLIM,0ohm,1/20W,0201,SMD,LF	C5874		AP_TEMP:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-02166 SIZE: D

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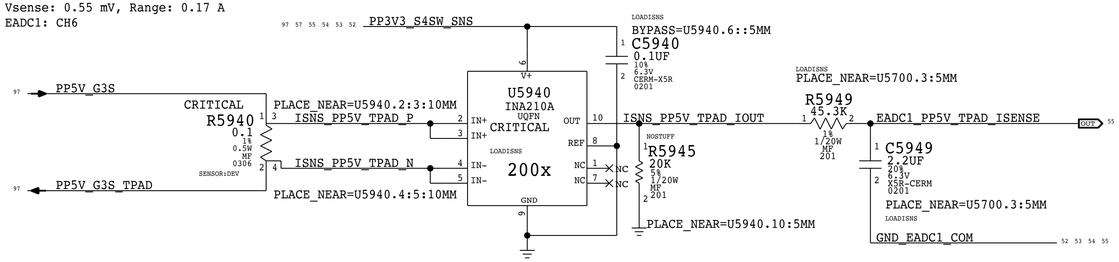
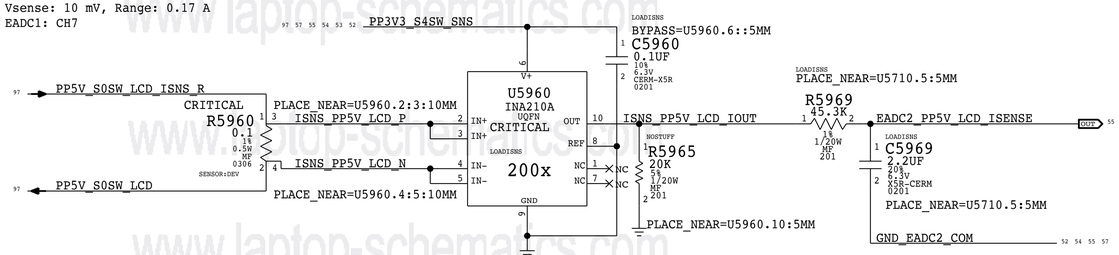
Trackpad 5V Current Sense (IT5C)

Gain: 200x, EDP: 0.0055 A
Rsense: 0.1 (R5940) or Rsense SHORT
Vsense: 0.55 mV, Range: 0.17 A
EADC1: CH6



LCD Panel 5V Current Sense (IL5C)

Gain: 200x, EDP: 0.1 A
Rsense: 0.1 (R5960) or Rsense SHORT
Vsense: 10 mV, Range: 0.17 A
EADC1: CH7



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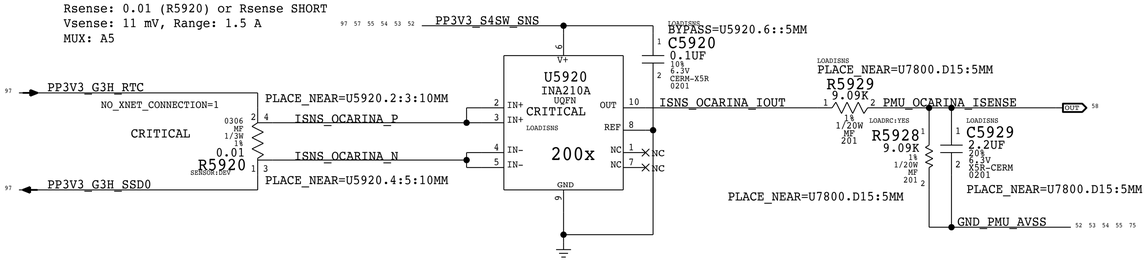
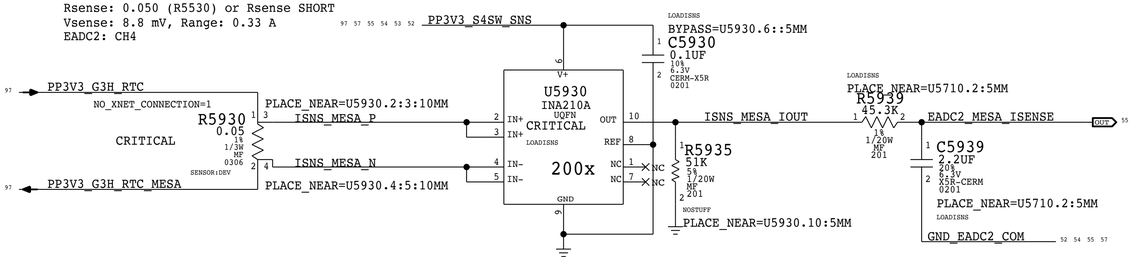
Ocarina Current Sense (IHCC)

Gain: 200x, EDP: 1.1 A
Rsense: 0.01 (R5920) or Rsense SHORT
Vsense: 11 mV, Range: 1.5 A
MUX: A5



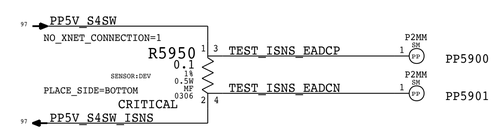
MESA Current Sense (IIDC)

Gain: 200x, EDP: 0.176 A
Rsense: 0.050 (R5530) or Rsense SHORT
Vsense: 8.8 mV, Range: 0.33 A
EADC2: CH4



EADC Current Sense

EDP: 6m A
Rsense: 0.1 (R5950) or Rsense SHORT
Vsense: 0.6 mV



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5928,R5958		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors:Extended 3

Apple Inc.

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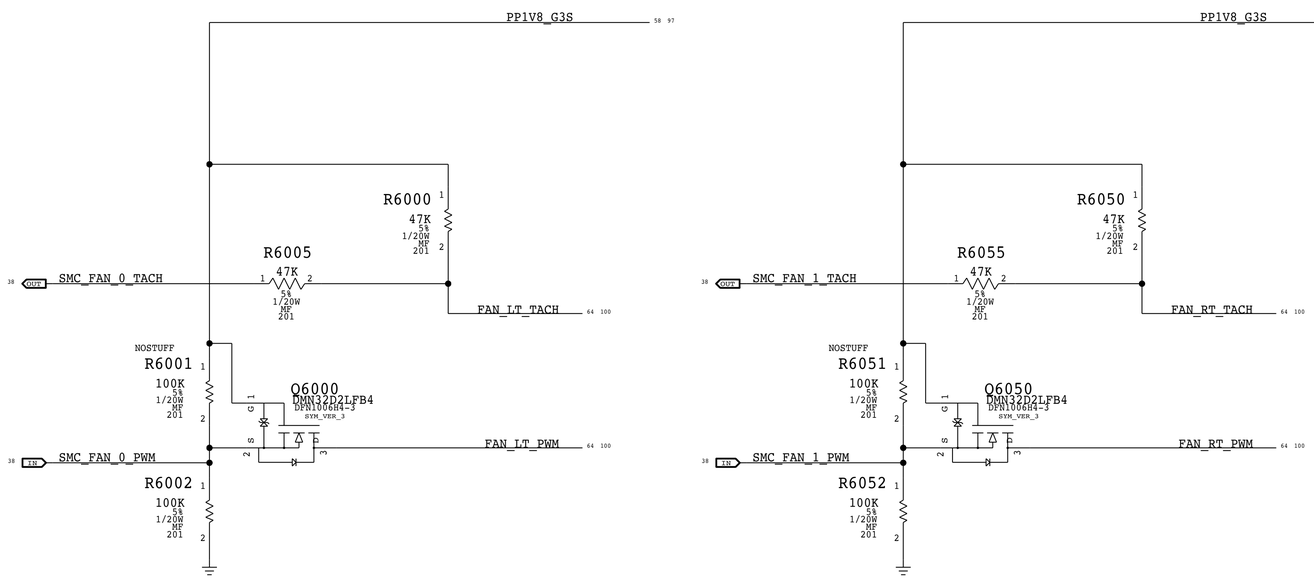
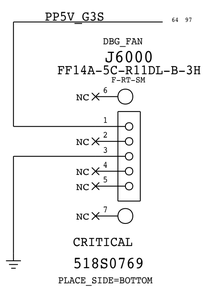
FAN CONTROL



FOR DEBUG FAN POWER



SMC ADC Assignments

52	IN	SMC_CPU_HS_ISENSE (MAKE_BASE=TRUE)	SMC_CPU_HS_ISENSE	OUT 38
52	IN	SMC_PBUS_VSENSE (MAKE_BASE=TRUE)	SMC_PBUS_VSENSE	OUT 38
52	IN	SMC_BMON_ISENSE (MAKE_BASE=TRUE)	SMC_BMON_ISENSE	OUT 38
52	IN	SMC_DCIN_ISENSE (MAKE_BASE=TRUE)	SMC_DCIN_ISENSE	OUT 38
52	IN	SMC_DCIN_VSENSE (MAKE_BASE=TRUE)	SMC_DCIN_VSENSE	OUT 38
53	IN	SMC_PP3V3_WLANBT_ISENSE (MAKE_BASE=TRUE)	SMC_PP3V3_WLANBT_ISENSE	OUT 38
53	IN	SMC_PP1V8_WLANBT_ISENSE (MAKE_BASE=TRUE)	SMC_PP1V8_WLANBT_ISENSE	OUT 38
55	IN	SMC_CALPE_ISENSE (MAKE_BASE=TRUE)	SMC_CALPE_ISENSE	OUT 38

KBL-U NB Assignments

CPUGT ISNS	ADC5
IACORE ISNS	ADC6

Desktop Assignments

GPU_AUX	ADC0
GPU_CORE	ADC1
12V VSNS	ADC2
12V ISNS	ADC3
Same	ADC4-7

PMU ADC Assignments

52	IN	PMU_OTHER3V3_HI_ISENSE (MAKE_BASE=TRUE)	PMU_OTHER3V3_HI_ISENSE	OUT 76
52	IN	PMU_OTHER5V_HI_ISENSE (MAKE_BASE=TRUE)	PMU_OTHER5V_HI_ISENSE	OUT 76
55	IN	PMU_CPUEDRAM_ISENSE (MAKE_BASE=TRUE)	PMU_CPUEDRAM_ISENSE	OUT 76
53	IN	PMU_CPUVCCIO_ISENSE (MAKE_BASE=TRUE)	PMU_CPUVCCIO_ISENSE	OUT 76
53	IN	PMU_DDR1V2_ISENSE (MAKE_BASE=TRUE)	PMU_DDR1V2_ISENSE	OUT 76
57	IN	PMU_OCARINA_ISENSE (MAKE_BASE=TRUE)	PMU_OCARINA_ISENSE	OUT 76
52	IN	PMU_SSDNAND_ISENSE (MAKE_BASE=TRUE)	PMU_SSDNAND_ISENSE	OUT 76
55	IN	PMU_CPUP5VREG_ISENSE (MAKE_BASE=TRUE)	PMU_CPUP5VREG_ISENSE	OUT 76
		NC_PMU_AMUX_AY (MAKE_BASE=TRUE)	NC_PMU_AMUX_AY	OUT 76
54	IN	PMU_LCDPANEL_ISENSE (MAKE_BASE=TRUE)	PMU_LCDPANEL_ISENSE	OUT 76
55	IN	PMU_CPUSA_ISENSE (MAKE_BASE=TRUE)	PMU_CPUSA_ISENSE	OUT 76
53	IN	PMU_CPUDDR_ISENSE (MAKE_BASE=TRUE)	PMU_CPUDDR_ISENSE	OUT 76
55	IN	PMU_CPUSA_VSENSE (MAKE_BASE=TRUE)	PMU_CPUSA_VSENSE	OUT 76
54	IN	PMU_CPU_VSENSE (MAKE_BASE=TRUE)	PMU_CPU_VSENSE	OUT 76
54	IN	PMU_CPUGT_VSENSE (MAKE_BASE=TRUE)	PMU_CPUGT_VSENSE	OUT 76
55	IN	PMU_CPUGT_ISENSE (MAKE_BASE=TRUE)	PMU_CPUGT_ISENSE	OUT 76
53	IN	PMU_CPU_ISENSE (MAKE_BASE=TRUE)	PMU_CPU_ISENSE	OUT 76
		NC_PMU_AMUX_BY (MAKE_BASE=TRUE)	NC_PMU_AMUX_BY	OUT 76

BOM_COST_GROUP=FAN

PAGE TITLE
Fans/SMC/AMUX Support

Apple Inc.

DRAWING NUMBER 051-02166
SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
PAGE 60 OF 150
SHEET 58 OF 108

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BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV MLB U
LAST CHANGE: Wed Feb 18 17:12:24 2015

SYNC_MASTER=J212_ADMIN SYNC_DATE=02/12/2015

PAGE TITLE

Audio Placeholder

Apple Inc.

DRAWING NUMBER	051-02166
SIZE	D
REVISION	4.0.0
BRANCH	evt-mars-0
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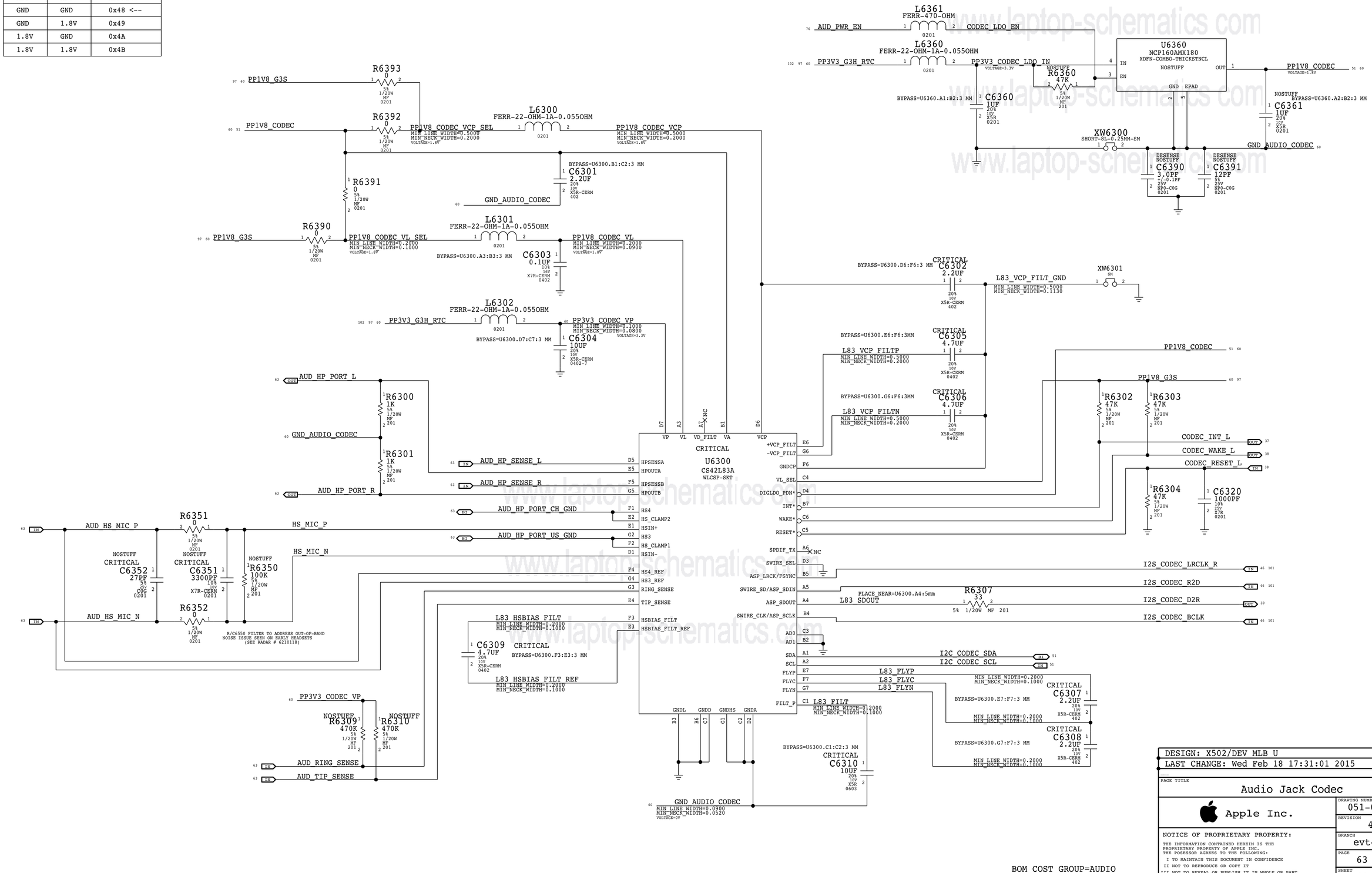
AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B



DESIGN: X502/DEV MLB U
LAST CHANGE: Wed Feb 18 17:31:01 2015

PAGE TITLE
Audio Jack Codec

Apple Inc.

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REVISION 4.0.0
BRANCH evt-mars-0
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SHEET 60 OF 108

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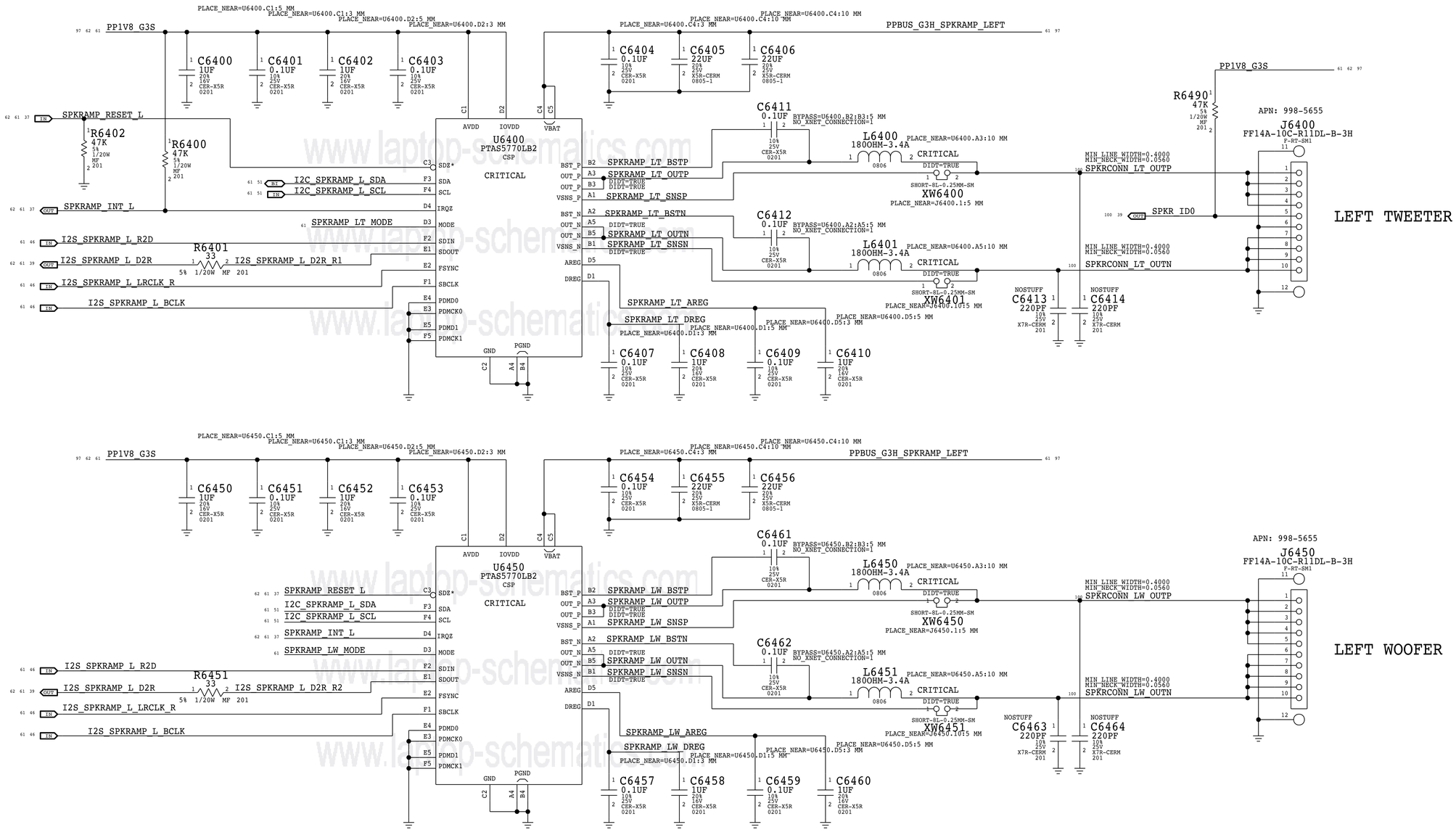
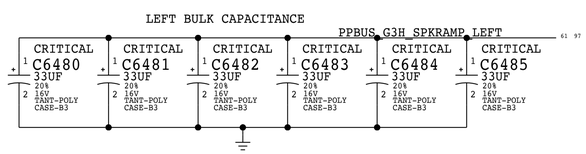
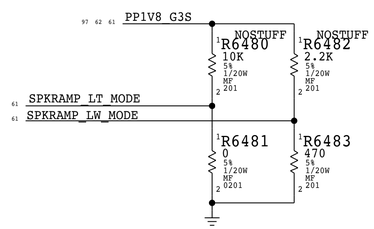
2X MONO SPEAKER LEFT AMPLIFIERS

APN: 353S01252
GAIN: 0DBFS = xxVRMS







MODE PIN	I2C ADDR	CHANNEL
GND	0x31	L TW
470 to GND	0x32	L WF
470 to IOVDD	0x33	R TW
2k2 to GND	0x34	R WF
2k2 to IOVDD	0x35	
10k to GND	0x36	
10k to IOVDD	0x37	
47k to IOVDD	0x38	

BOM_COST_GROUP=AUDIO

PAGE TITLE
Audio Left Amplifiers

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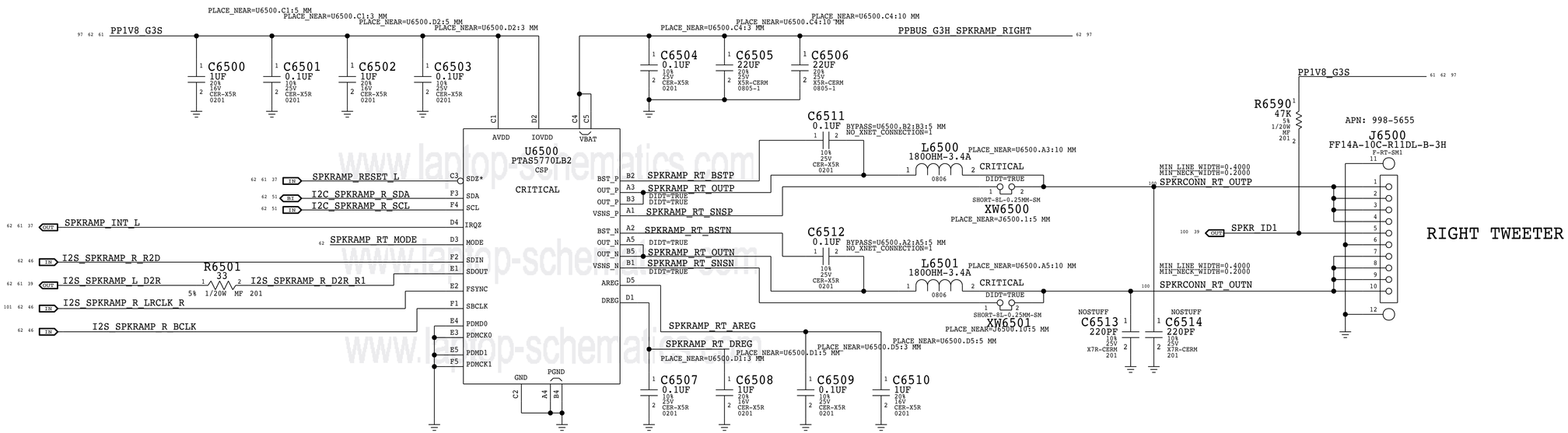
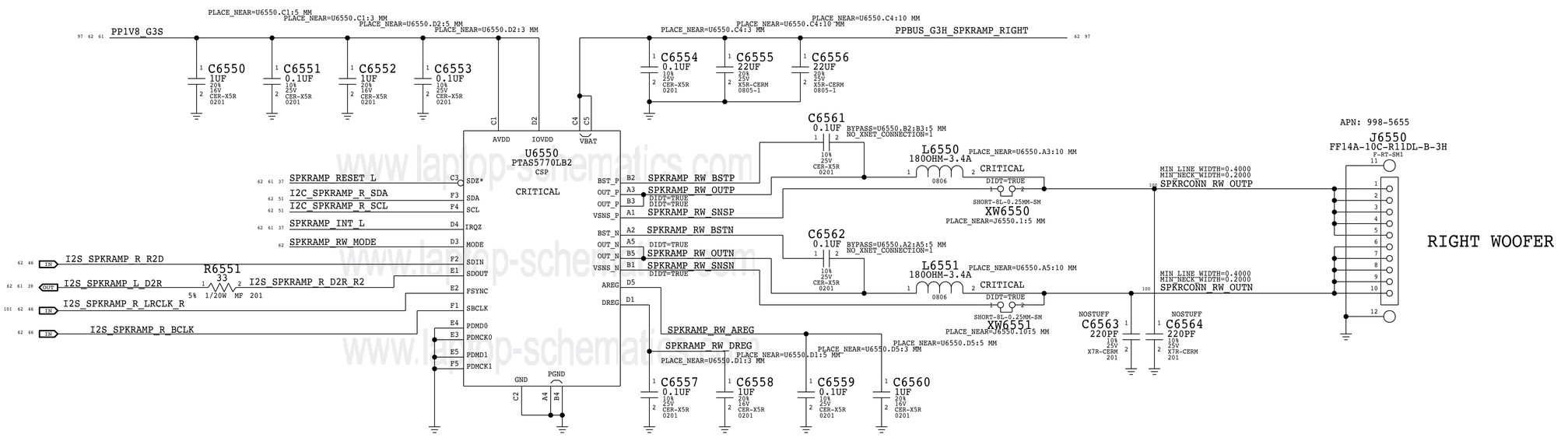
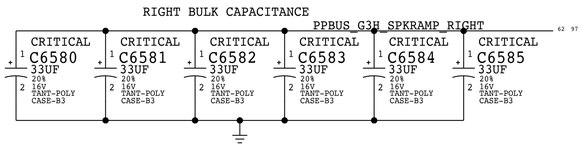
REVISION 4.0.0
BRANCH evt-mars-0
PAGE 64 OF 150
SHEET 61 OF 108

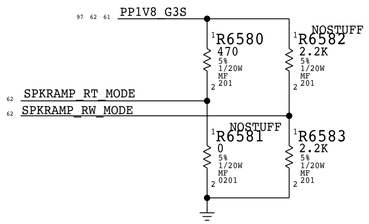
2X MONO SPEAKER RIGHT AMPLIFIERS

APN: 353S01252
GAIN: 0DBFS = xxVRMS









MODE PIN	I2C ADDR	CHANNEL
GND	0x31	L TW
470 to GND	0x32	L WF
470 to IOVDD	0x33	R TW
2k2 to GND	0x34	R WF
2k2 to IOVDD	0x35	
10k to GND	0x36	
10k to IOVDD	0x37	
47k to IOVDD	0x38	

BOM_COST_GROUP=AUDIO

PAGE TITLE
Audio Right Amplifiers

Apple Inc.

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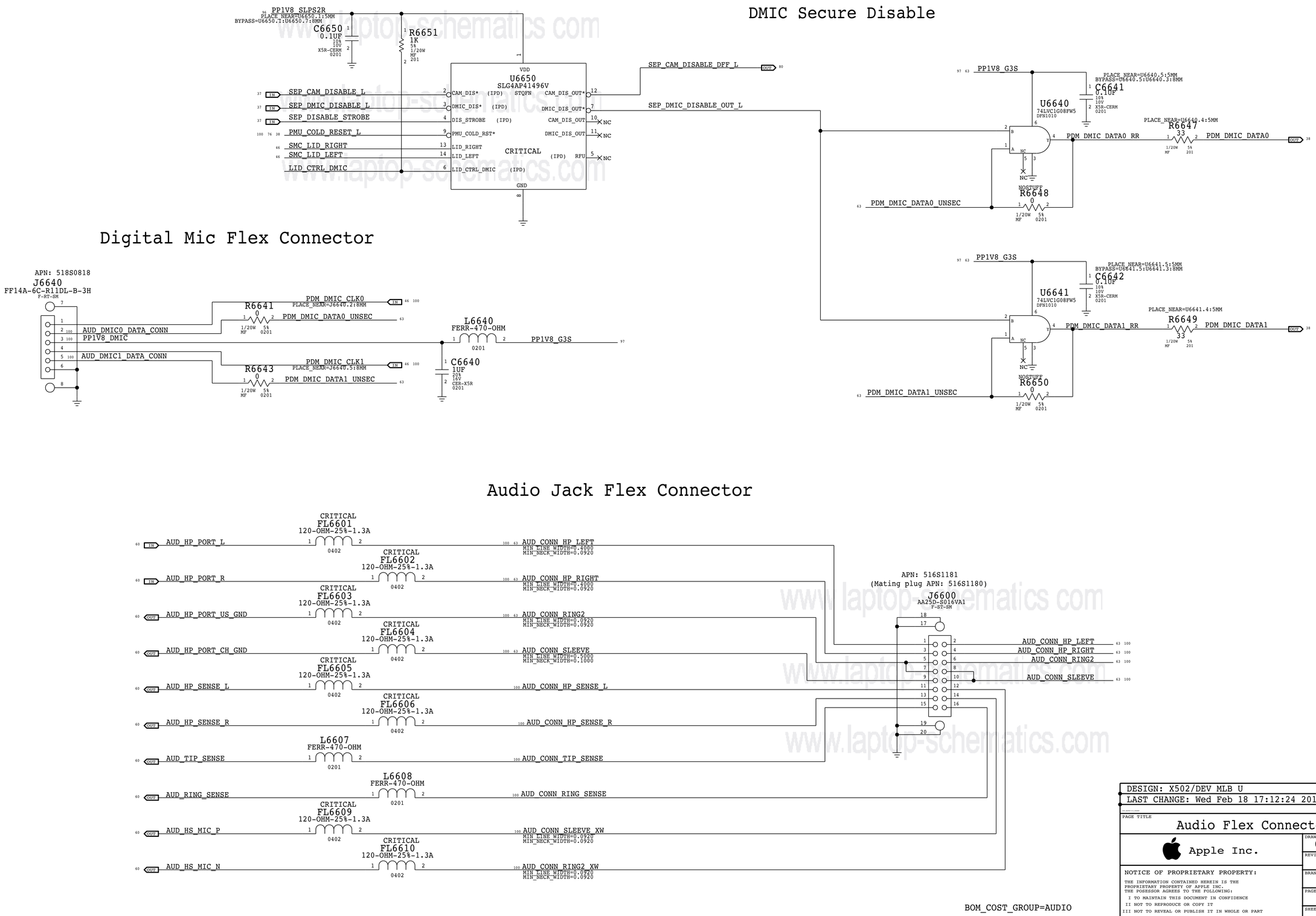

DESIGN: X502/DEV MLB U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
Audio Flex Connectors

Apple Inc.

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BRANCH evt-mars-0
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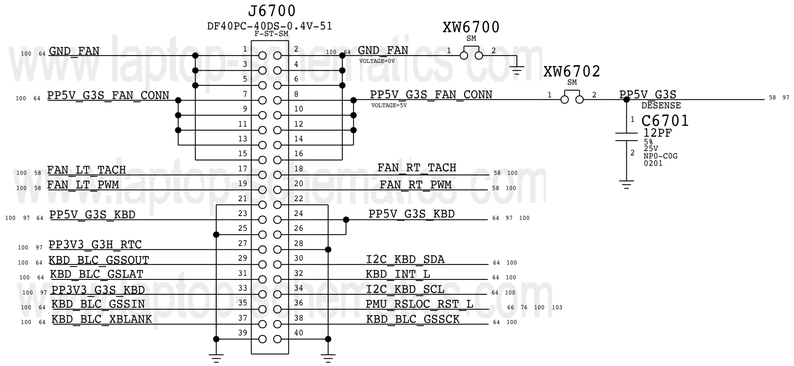
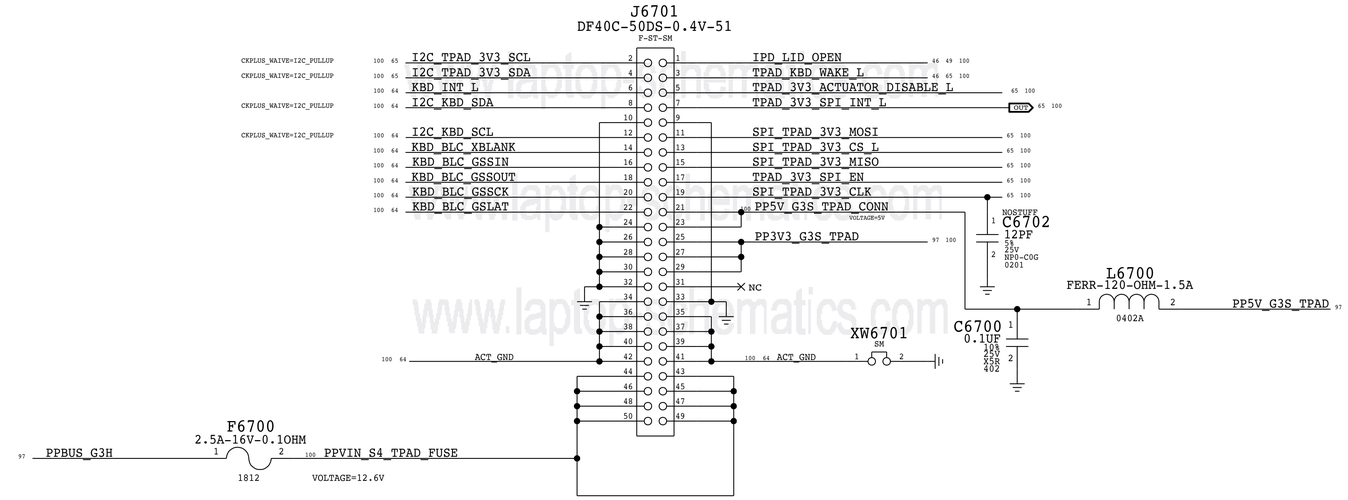
KBD CONNECTOR



516S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

TPAD CONNECTOR



516S00187, MATE WITH 516S00188

BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=J132_GAMER SYNC_DATE=04/12/2017

PAGE TITLE
Keyboard & Trackpad 1

Apple Inc.

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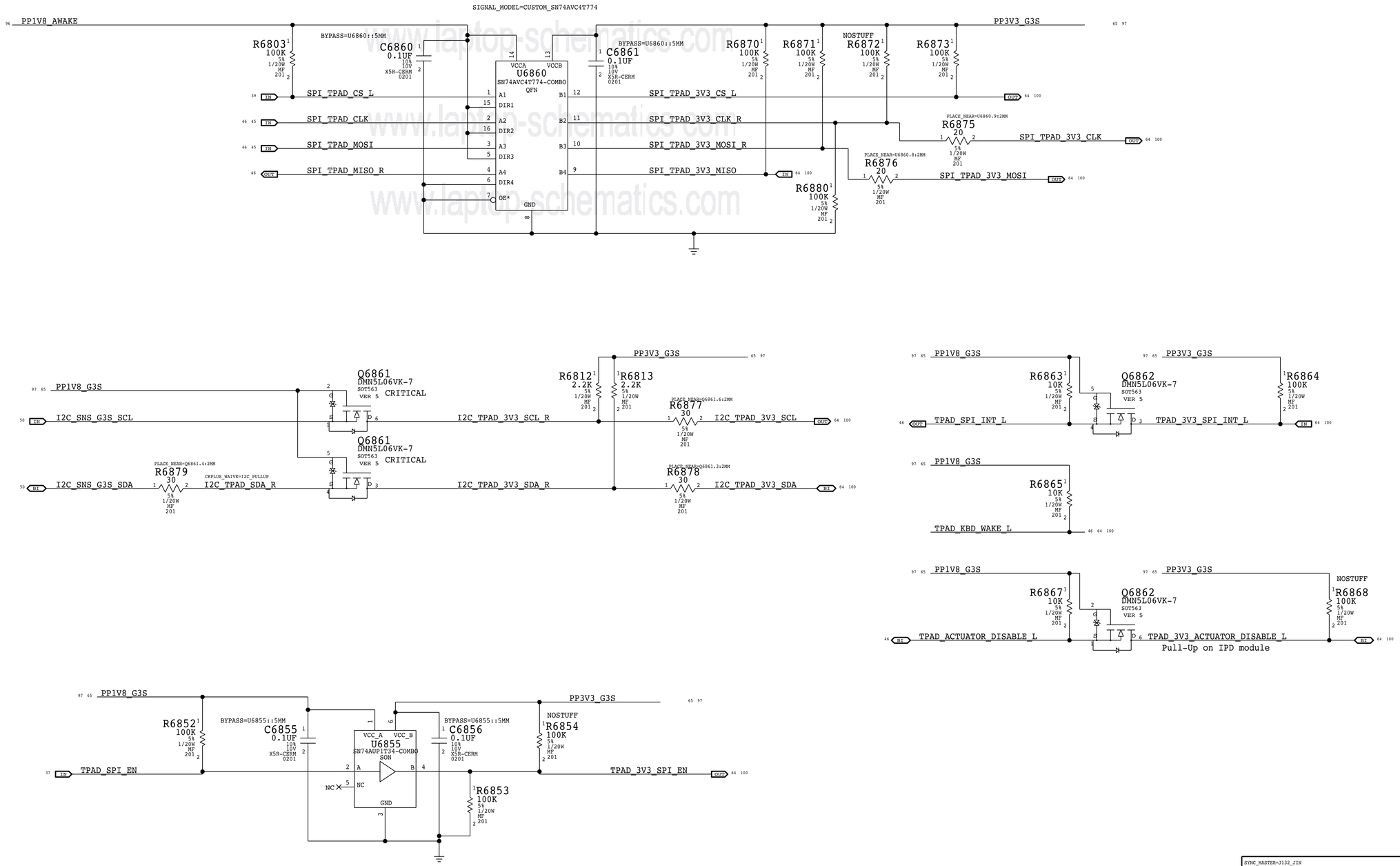
Trackpad Level Shifting



BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=J132_JIN SYNC_DATE=09/05/2017

PAGE TITLE

Keyboard & Trackpad 2

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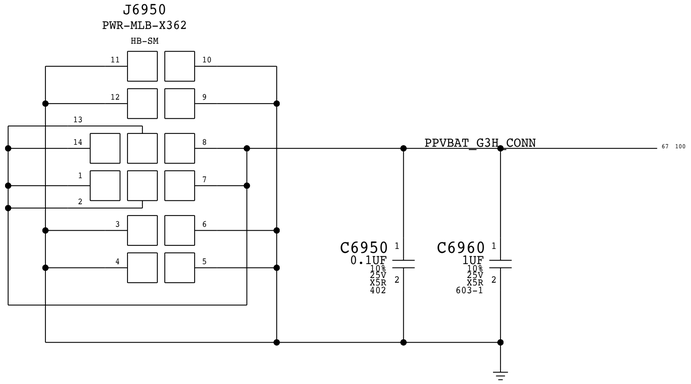
J79 Battery Hotbar Flex Pads



BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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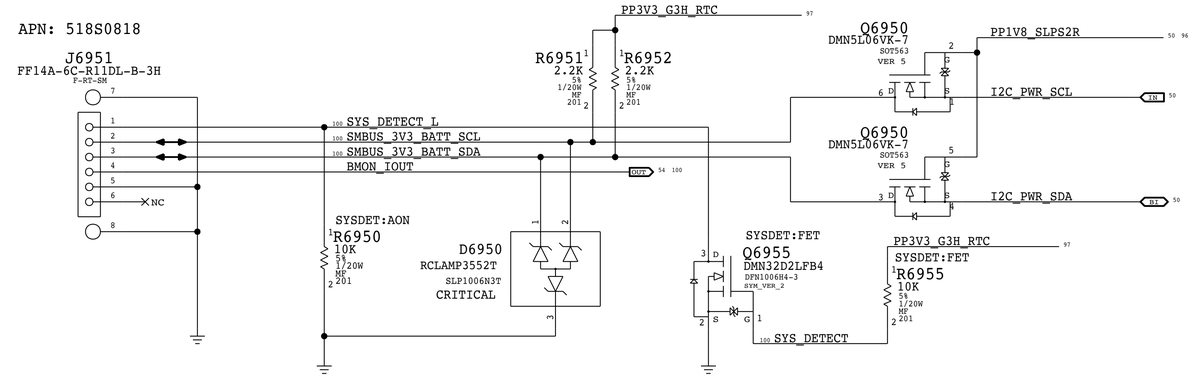
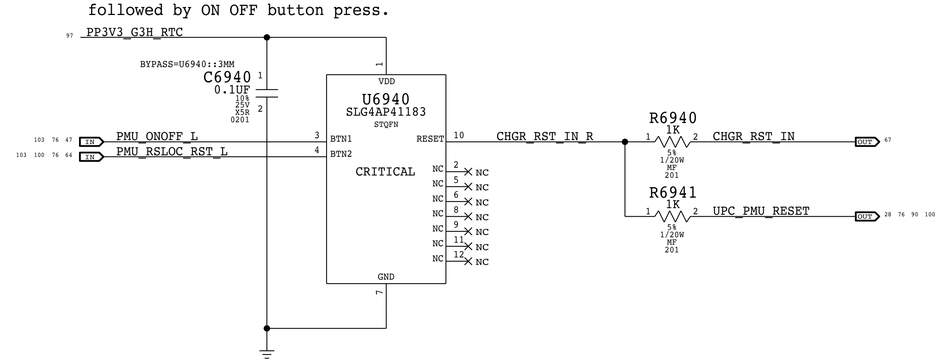
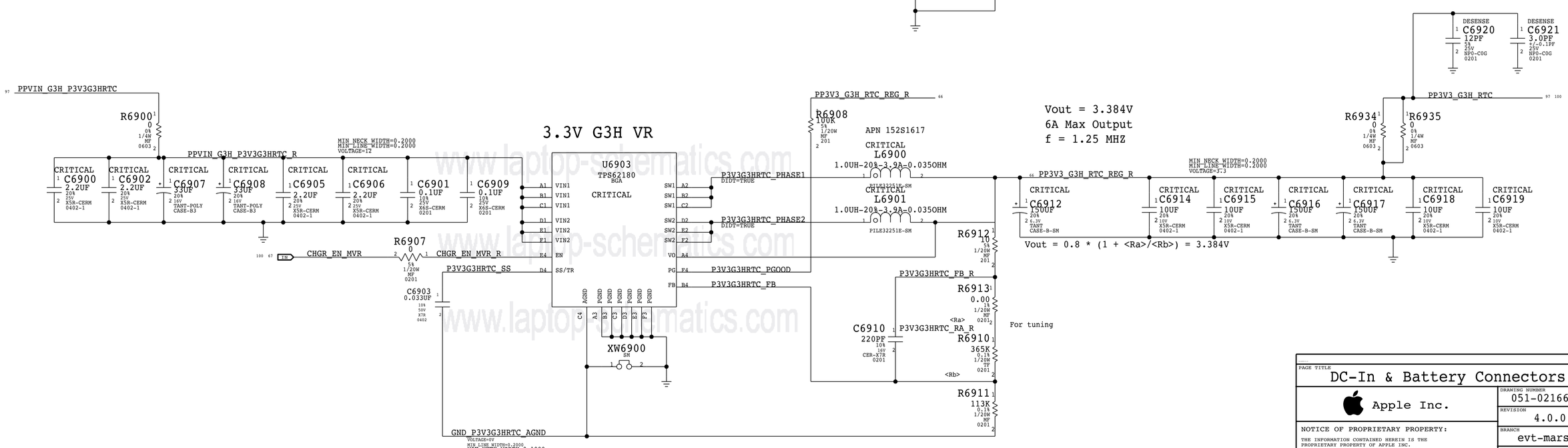


SMC Reset Circuit

Right Shift & Left Option Control
followed by ON OFF button press.





BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

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BRANCH evt-mars-0
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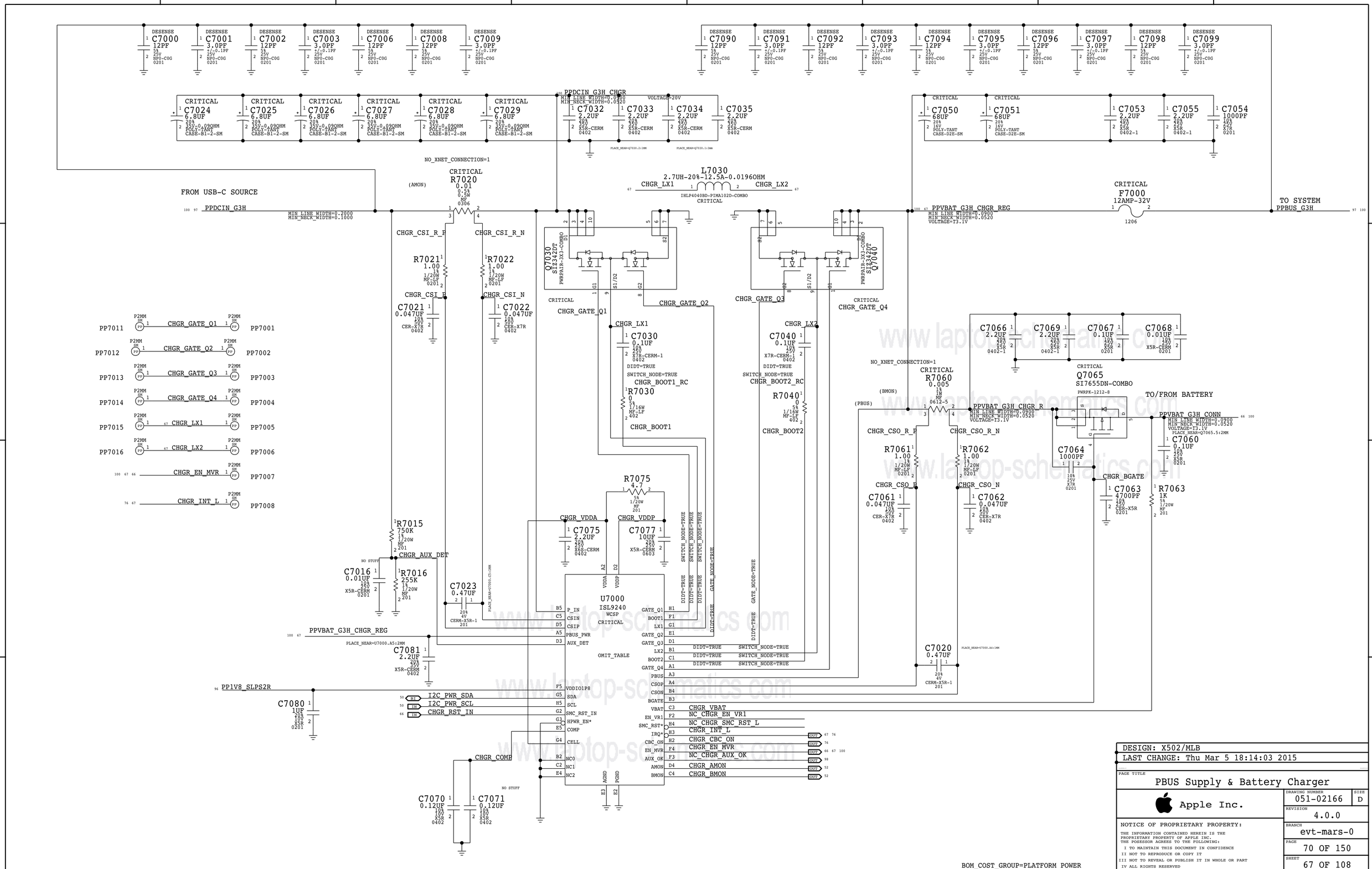

DESIGN: X502/MLB
LAST CHANGE: Thu Mar 5 18:14:03 2015

PAGE TITLE
PBUS Supply & Battery Charger

Apple Inc.

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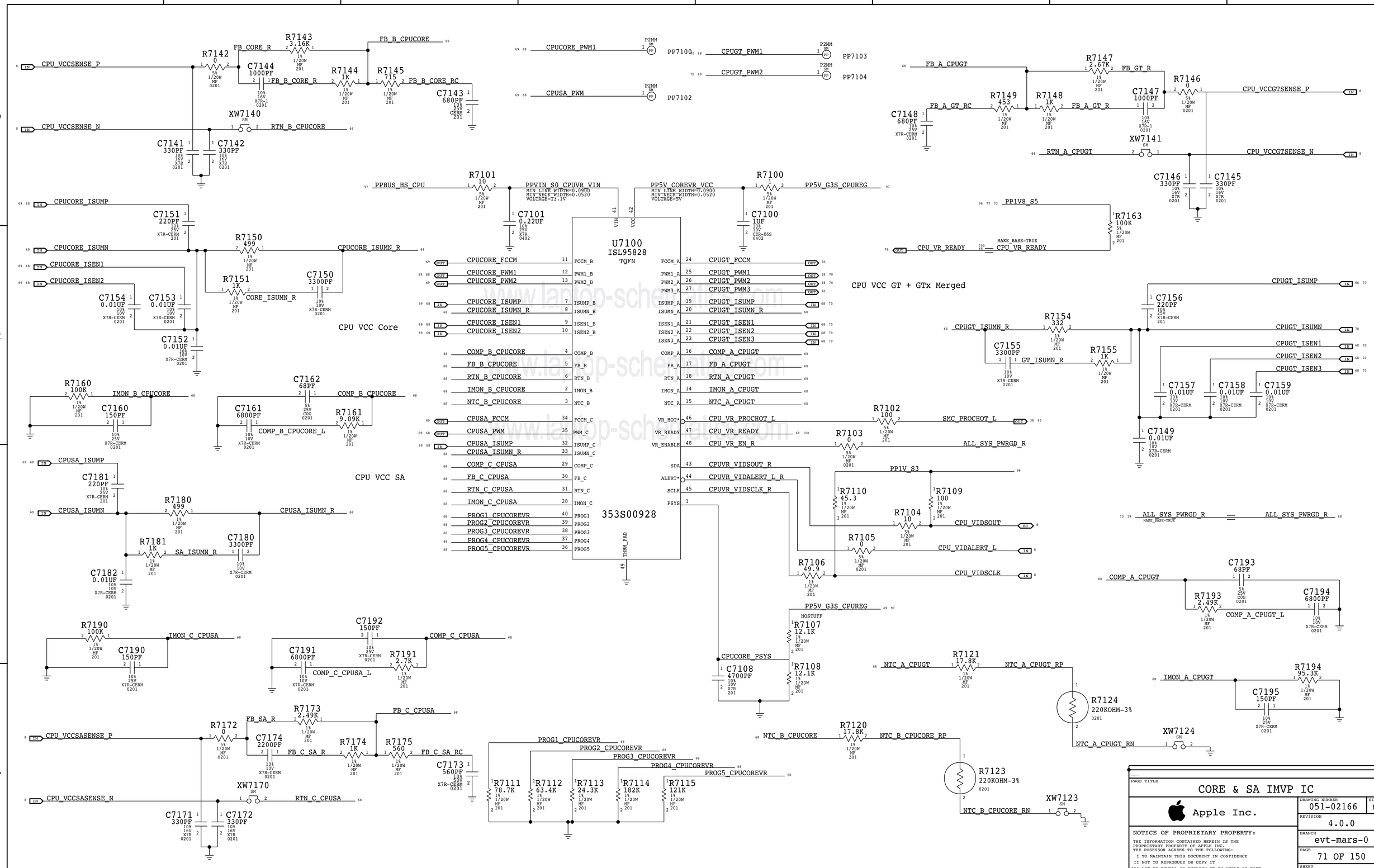
CPU_VCCSENSE_P
CPU_VCCSENSE_N
R7142 0
C7144 1000PF
R7143 3.16K
R7144 1K
R7145 715
FB_CORE_R
FB_B_CPUCORE
FB_B_CORE_R
FB_B_CORE_RC
C7143 680PF
XW7140
RTN_B_CPUCORE
C7141 330PF
C7142 330PF
CPUCORE_PWM1
CPUSA_PWM
PP7100
PP7102
CPUGT_PWM1
CPUGT_PWM2
PP7103
PP7104
FB_A_CPUGT
R7147 2.67K
FB_GT_R
R7146 0
CPU_VCCGTSENSE_P
C7148 680PF
FB_A_GT_RC
R7149 453
R7148 1K
FB_A_GT_R
C7147 1000PF
XW7141
RTN_A_CPUGT
CPU_VCCGTSENSE_N
C7146 330PF
C7145 330PF
PPBUS_HS_CPU
R7101 10
PPVIN_S0_CPUVR_VIN
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
C7101 0.22UF
PP5V_COREVR_VCC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
R7100 1
PP5V_G3S_CPUREG
C7100 1UF
PP1V8_S5
R7163 100K
CPU_VR_READY
MAKE_BASE=TRUE
CPUCORE_ISUMP
C7151 220PF
CPUCORE_ISUMN
R7150 499
CPUCORE_ISUMN_R
CPUCORE_ISEN1
CPUCORE_ISEN2
C7154 0.01UF
C7153 0.01UF
R7151 1K
CORE_ISUMN_R
C7150 3300PF
C7152 0.01UF
CPU VCC Core
U7100
ISL95828
TQFN
353S00928
THRM_PAD
CPUCORE_FCCM
CPUCORE_PWM1
CPUCORE_PWM2
CPUCORE_ISUMP
CPUCORE_ISUMN_R
CPUCORE_ISEN1
CPUCORE_ISEN2
COMP_B_CPUCORE
FB_B_CPUCORE
RTN_B_CPUCORE
IMON_B_CPUCORE
NTC_B_CPUCORE
CPUSA_FCCM
CPUSA_PWM
CPUSA_ISUMP
CPUSA_ISUMN_R
COMP_C_CPUSA
FB_C_CPUSA
RTN_C_CPUSA
IMON_C_CPUSA
PROG1_CPUCOREVR
PROG2_CPUCOREVR
PROG3_CPUCOREVR
PROG4_CPUCOREVR
PROG5_CPUCOREVR
CPUGT_FCCM
CPUGT_PWM1
CPUGT_PWM2
CPUGT_PWM3
CPUGT_ISUMP
CPUGT_ISUMN_R
CPUGT_ISEN1
CPUGT_ISEN2
CPUGT_ISEN3
COMP_A_CPUGT
FB_A_CPUGT
RTN_A_CPUGT
IMON_A_CPUGT
NTC_A_CPUGT
CPU_VR_PROCHOT_L
CPU_VR_READY
CPU_VR_EN_R
CPUVR_VIDSOUT_R
CPUVR_VIDALERT_L_R
CPUVR_VIDSCLK_R
CPU VCC GT + GTx Merged
R7102 100
SMC_PROCHOT_L
R7103 0
ALL_SYS_PWRGD_R
PP1V_S3
R7110 45.3
R7109 100
R7104 10
CPU_VIDSOUT
R7105 0
CPU_VIDALERT_L
R7106 49.9
CPU_VIDSCLK
C7156 220PF
CPUGT_ISUMP
CPUGT_ISUMN_R
R7154 332
C7155 3300PF
GT_ISUMN_R
R7155 1K
CPUGT_ISUMN
CPUGT_ISEN1
CPUGT_ISEN2
CPUGT_ISEN3
C7157 0.01UF
C7158 0.01UF
C7159 0.01UF
C7149 0.01UF
R7160 100K
IMON_B_CPUCORE
C7160 150PF
C7162 68PF
C7161 6800PF
COMP_B_CPUCORE_L
R7161 9.09K
CPU VCC SA
C7181 220PF
R7180 499
CPUSA_ISUMN_R
R7181 1K
SA_ISUMN_R
C7180 3300PF
C7182 0.01UF
C7193 68PF
R7193 2.49K
COMP_A_CPUGT_L
C7194 6800PF
PP5V_G3S_CPUREG
NOSTUFF
R7107 12.1K
CPUCORE_PSYS
C7108 4700PF
R7108 12.1K
R7190 100K
IMON_C_CPUSA
C7190 150PF
C7192 150PF
C7191 6800PF
COMP_C_CPUSA_L
R7191 2.7K
R7121 17.8K
NTC_A_CPUGT
NTC_A_CPUGT_RP
R7124 220KOHM-3%
NTC_A_CPUGT_RN
R7194 95.3K
C7195 150PF
XW7124
R7173 2.49K
FB_SA_R
FB_C_CPUSA
R7172 0
CPU_VCCSASENSE_P
C7174 2200PF
FB_C_SA_R
R7174 1K
R7175 560
FB_C_SA_RC
C7173 560PF
XW7170
CPU_VCCSASENSE_N
RTN_C_CPUSA
C7171 330PF
C7172 330PF
PROG1_CPUCOREVR
PROG2_CPUCOREVR
PROG3_CPUCOREVR
PROG4_CPUCOREVR
PROG5_CPUCOREVR
R7111 78.7K
R7112 63.4K
R7113 24.3K
R7114 182K
R7115 121K
R7120 17.8K
NTC_B_CPUCORE
NTC_B_CPUCORE_RP
R7123 220KOHM-3%
NTC_B_CPUCORE_RN
XW7123
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CORE & SA IMVP IC
Apple Inc.
DRAWING NUMBER 051-02166
SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
PAGE 71 OF 150
SHEET 68 OF 108
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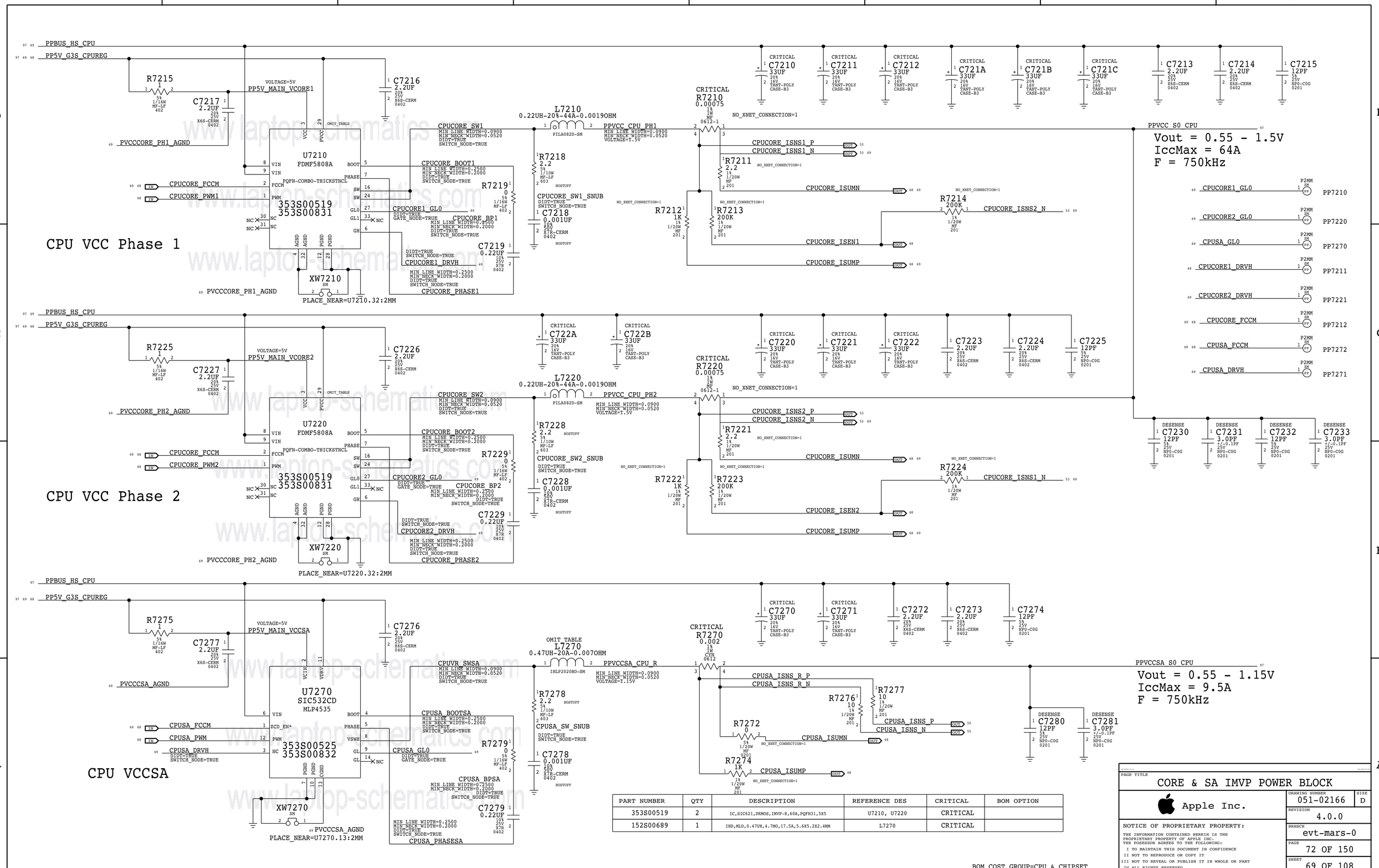

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00519	2	IC,SIC621,DRMOS,IMVP-8,60A,PQFN31,5X5	U7210, U7220	CRITICAL	
152S00689	1	IND,MLD,0.47UH,4.7MO,17.5A,5.6X5.2X2.4MM	L7270	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CORE & SA IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-02166 SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
PAGE 72 OF 150
SHEET 69 OF 108

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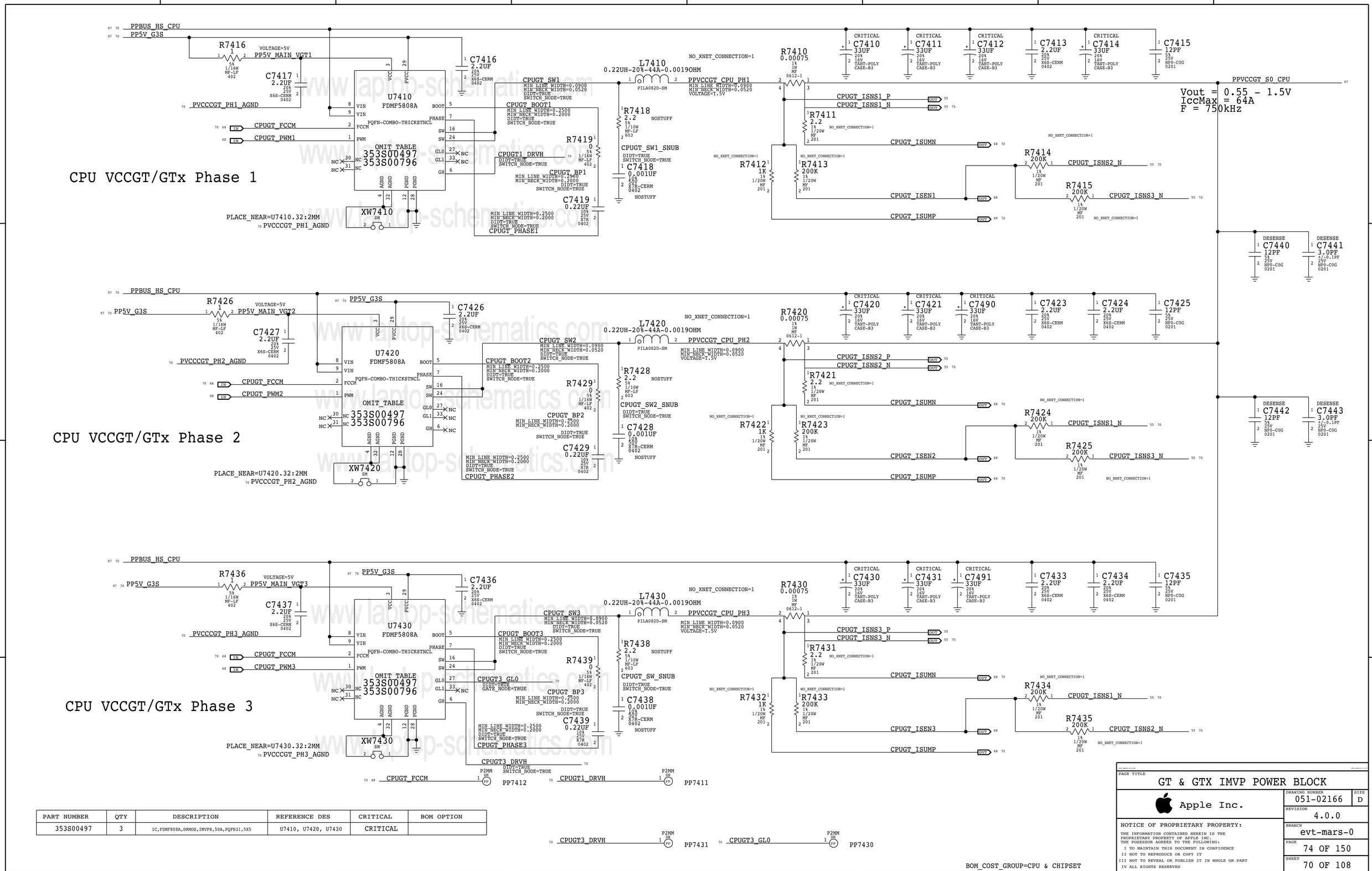

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,FDMF808A,DRMOS,IMVP8,50A,PQFN31,5X5	U7410, U7420, U7430	CRITICAL	

PAGE TITLE

GT & GTX IMVP POWER BLOCK

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SYNC_MASTER=J132_MAO SYNC_DATE=02/09/2017

PAGE TITLE

Empty

Apple Inc.

DRAWING NUMBER	051-02166
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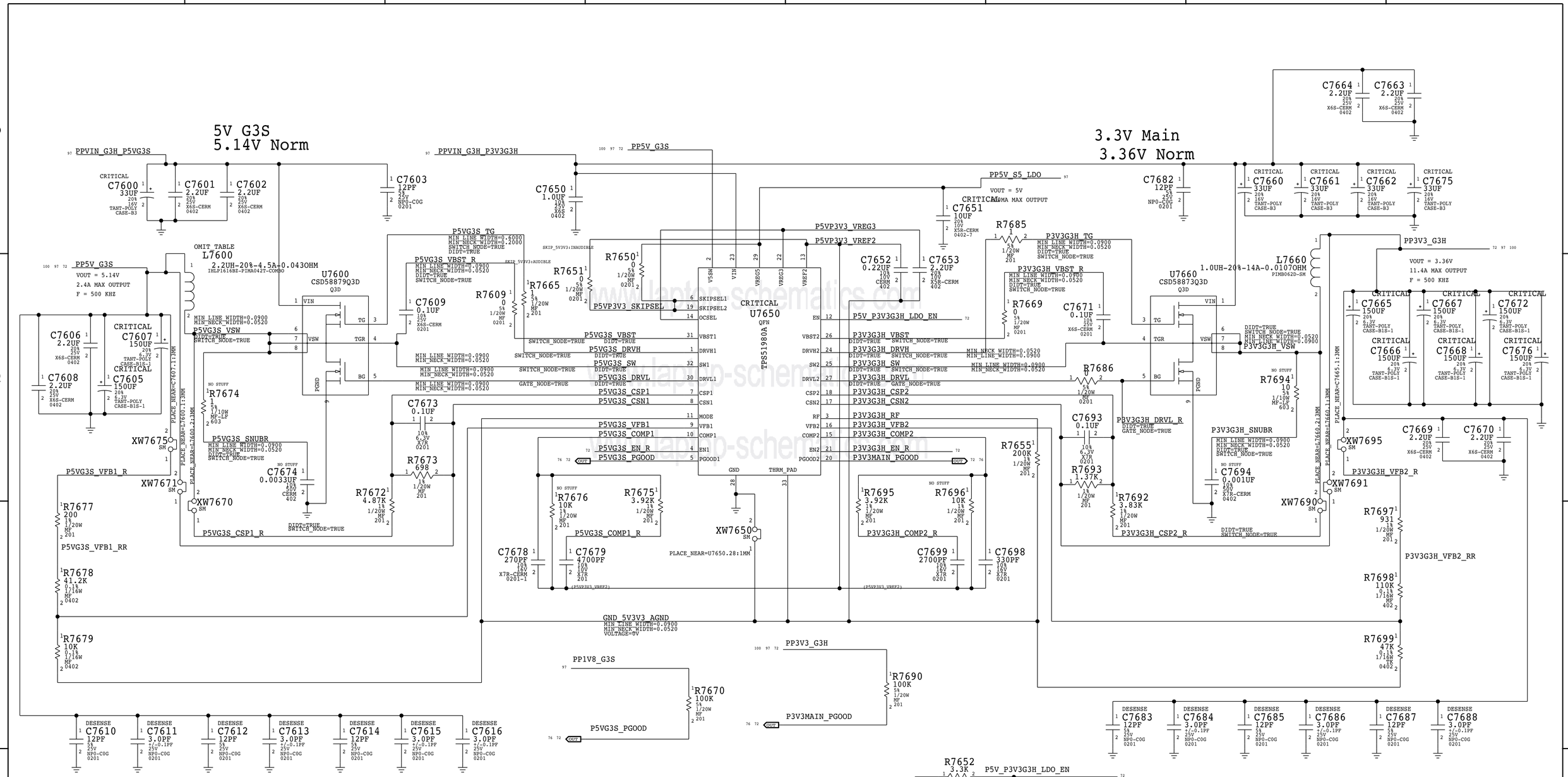

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00182	1	IND,PWR,2.2UH,20%,4.5A,43MOHM,4X4MM	L7600	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power - 5V 3.3V Supply

Apple Inc.

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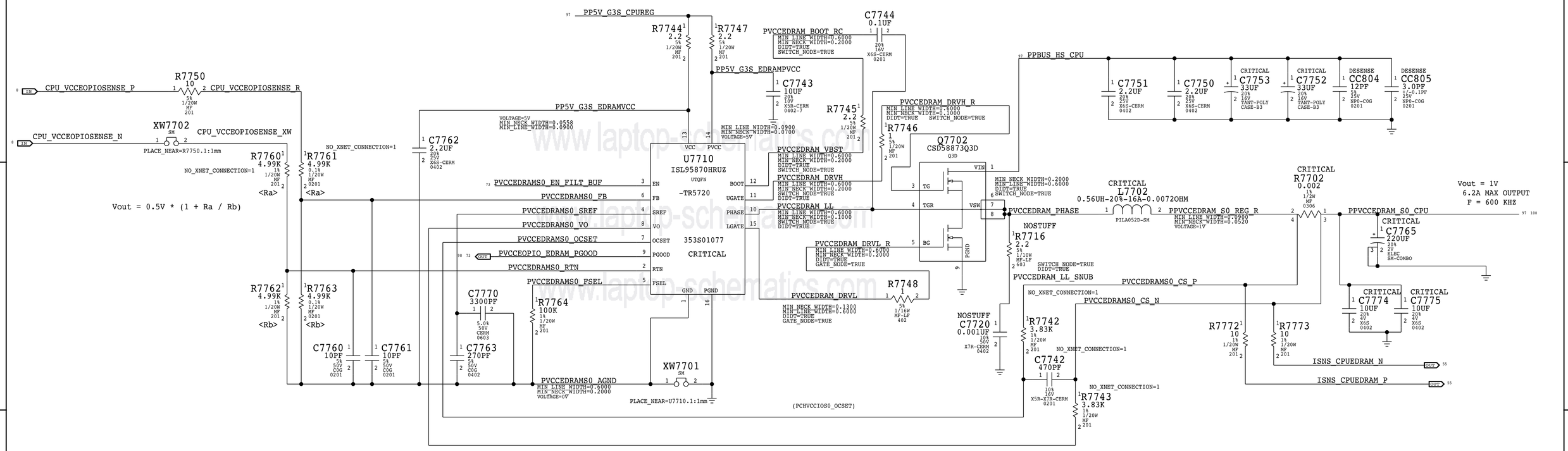
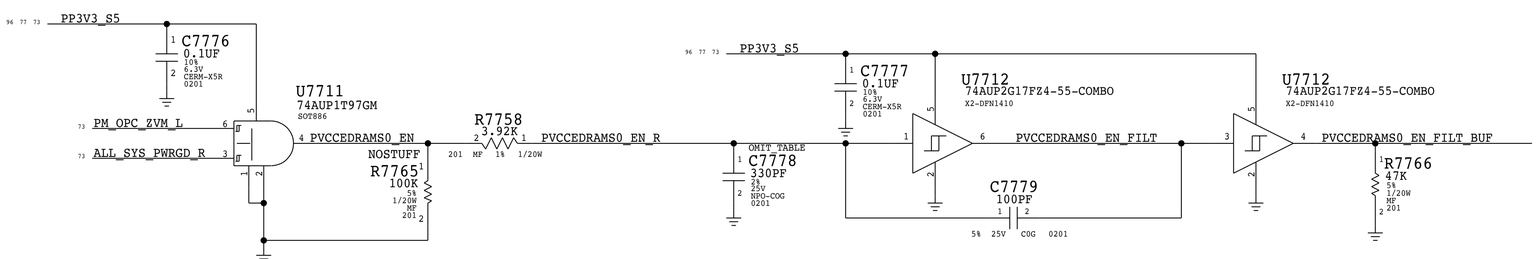
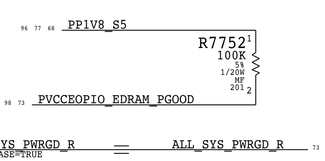
1V EDRAM & EOPIO



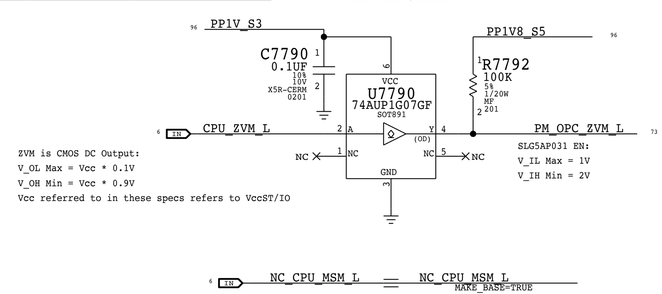


EDRAM EN BYPASS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00294	1	CAP,C0G,330PF,5%,25V,0201	C7778		



LEVEL SHIFT



ZVM is CMOS DC Output:
V_OL Max = Vcc * 0.1V
V_OH Min = Vcc * 0.9V
Vcc referred to in these specs refers to VccST/IO

SLG5AP031 EN:
V_IL Max = 1V
V_IH Min = 2V

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Power - EOPIO EDRAM Supply

Apple Inc.

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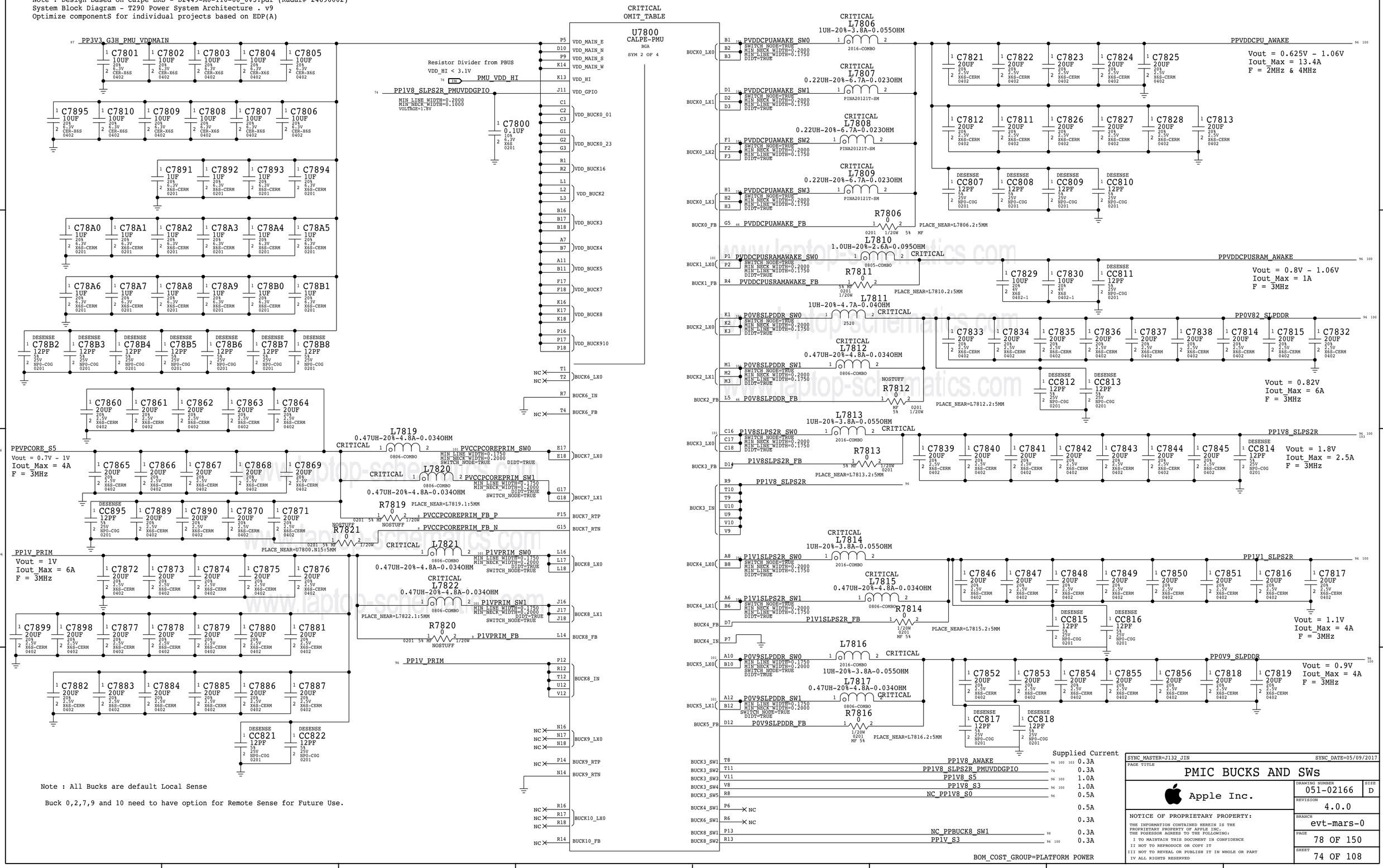
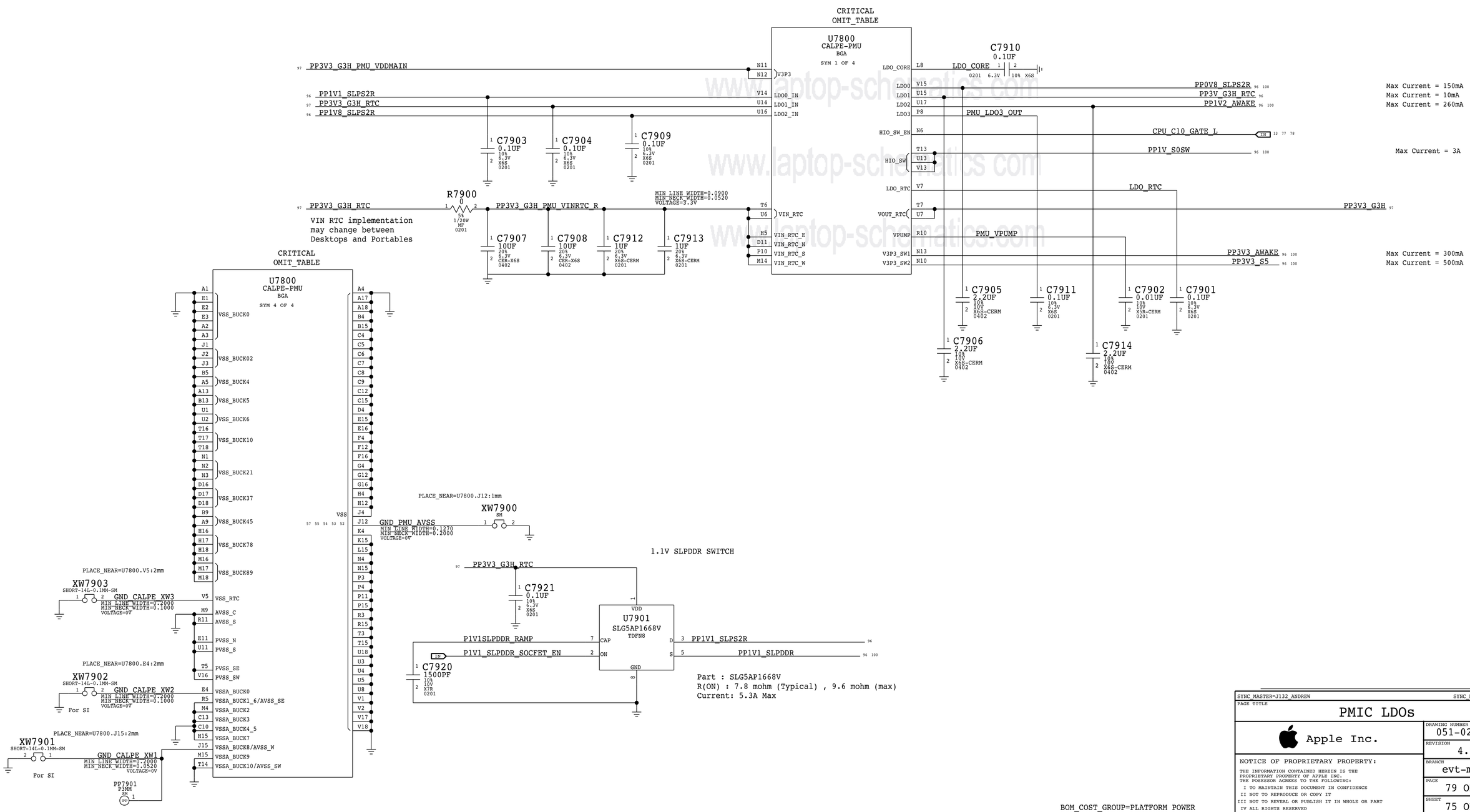
Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)





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SYNC_MASTER=J132_ANDREW SYNC_DATE=06/21/2017

PAGE TITLE

PMIC LDOs

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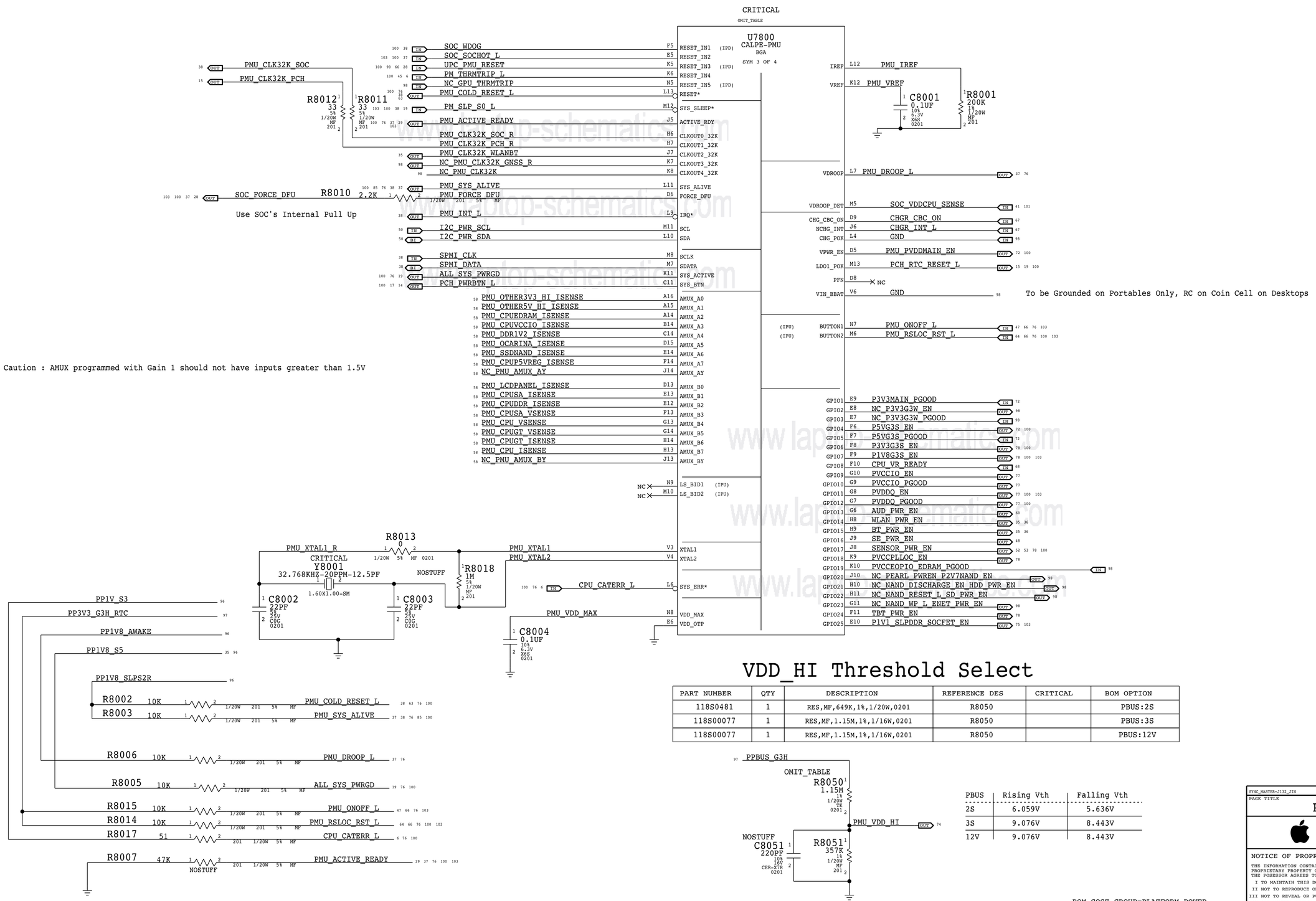

VDD_HI Threshold Select

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0481	1	RES,MF,649K,1%,1/20W,0201	R8050		PBUS:2S
118S00077	1	RES,MF,1.15M,1%,1/16W,0201	R8050		PBUS:3S
118S00077	1	RES,MF,1.15M,1%,1/16W,0201	R8050		PBUS:12V

PBUS	Rising Vth	Falling Vth
2S	6.059V	5.636V
3S	9.076V	8.443V
12V	9.076V	8.443V

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J132_JIN SYNC_DATE=09/05/2017

PAGE TITLE

PMIC GPIOs & Control

Apple Inc.

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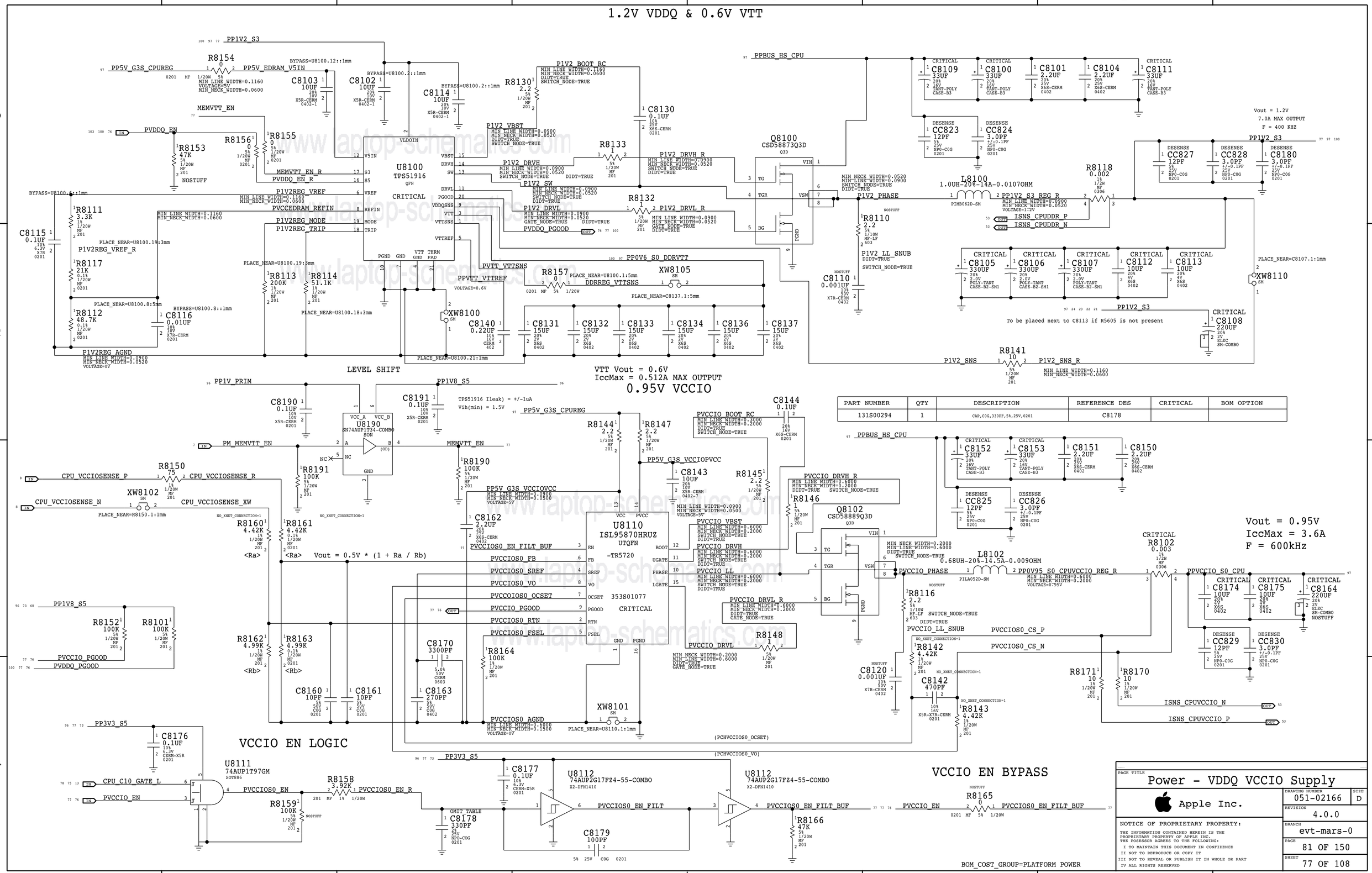

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00294	1	CAP,C0G,330PF,5%,25V,0201	C8178		

PAGE TITLE

Power - VDDQ VCCIO Supply

Apple Inc.

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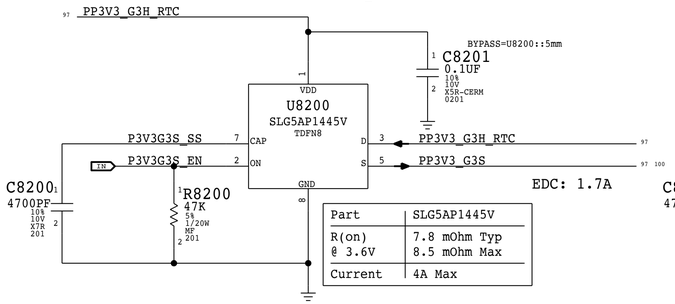
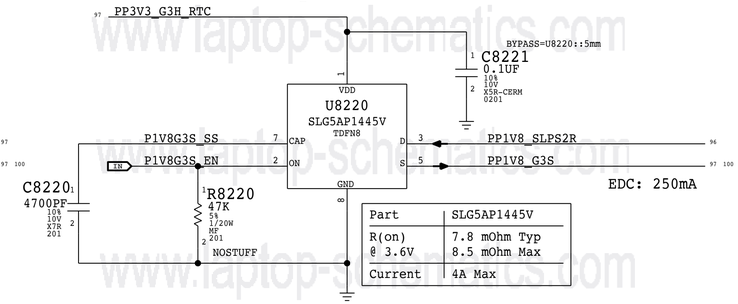
Note: Load switches may be larger than necessary

3.3V G3 Standby Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

1.8V G3 Standby Switch



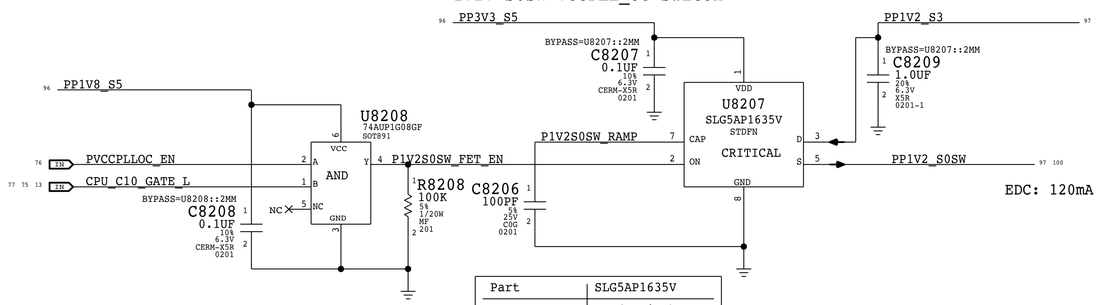
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

System Power States

System State:	Shutdown (G3H)		Standby (G3S)		Standby (S4)		Sleep (S0i/S3)		Run (S0)
CPU/PCH State:	Off (RTC Only)		Off (RTC Only)		Standby		Sleep		Run
Rails / SoC State:	S2R	Awake	S2R	Awake	S2R	Awake	S2R	Awake	Awake
PP*_S2R (0.8,1.1,1.8V)	On	On	On	On	On	On	On	On	On
PP*_DDR (0.8,0.9,1.1V)	Off	On	Off	On	Off	On	Off	On	On
PP*_AWAKE (CPU,SRAM,1.2,1.8,3.3V)	Off	On	Off	On	Off	On	Off	On	On
PP3V3_G3H (VR1)	On	On	On	On	On	On	On	On	On
PP*_G3S (1.8,3.3,5V)	Off	On	On	On	On	On	On	On	On
PP*_S5 (1.8,3.3V)	Off	Off	Off	Off	On	On	On	On	On
CPU/PCH VRs	Off	Off	Off	Off	Off/On	Off/On	Off/On	Off/On	On

* System: Shutdown Awake is a transition state only.
* SoC: SLP_DDR is a transition state only.
* CPU/PCH: S4 is only used by desktops for USB wakes.
* CPU/PCH: S5 is a transition state. May also be used for RTC wakes.

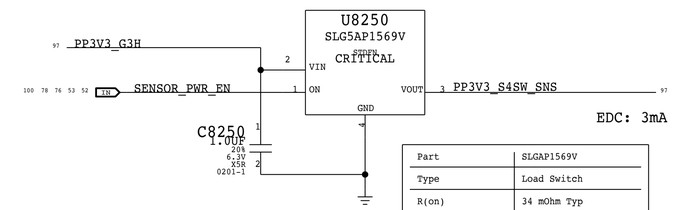
1.2V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.3V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

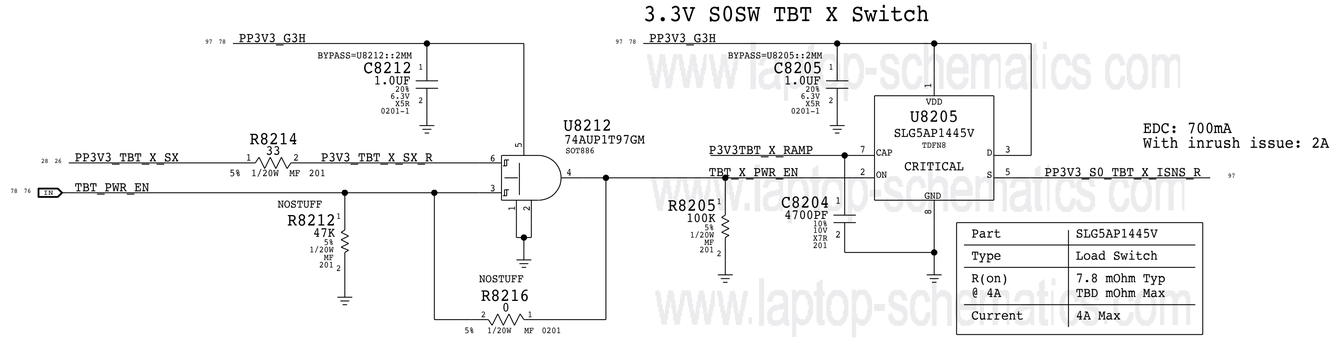
VCCPLL_OC has turn-on requirement of 11uS min and 240uS max from EN to 1.1V

3.3V Sensor Switch



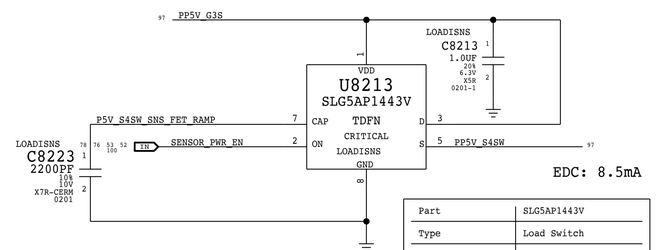
Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

3.3V S0SW TBT X Switch



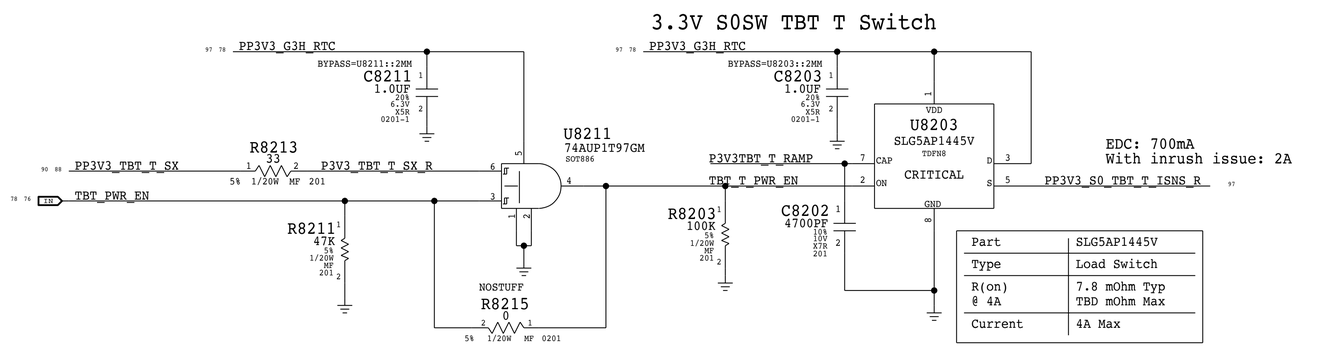
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

5V Sensor Switch



Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

3.3V S0SW TBT T Switch



Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J132_J18 SYNC_DATE=09/05/2017

PAGE TITLE

Power FETs

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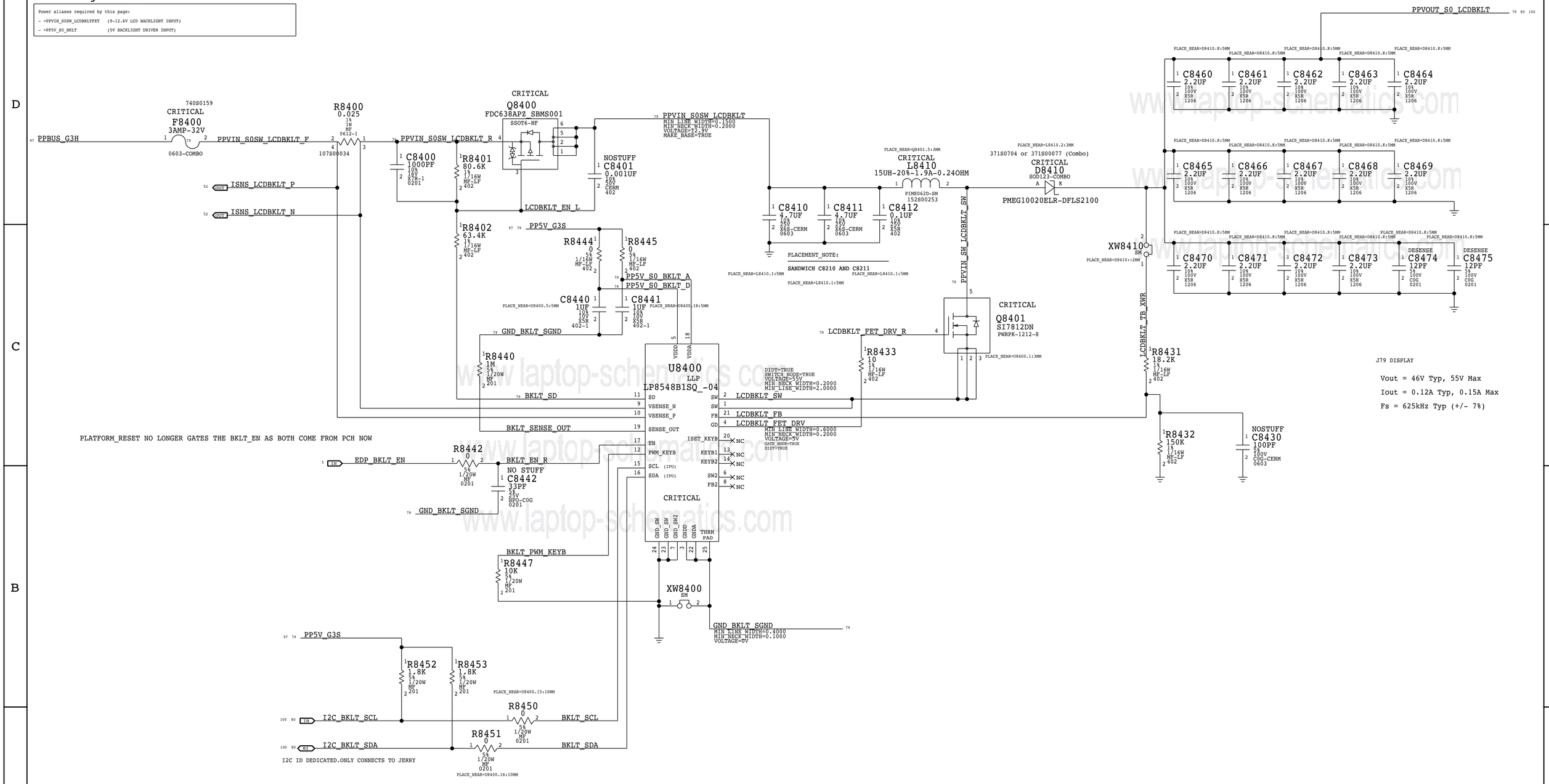
Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



LINE WIDTHS

PP5V_S0_BKLT_A
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

PP5V_S0_BKLT_D
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

BKLT_SD
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000

PBUS LINE WIDTHS

PPVIN_S0SW_LCDBKLT_F
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_R
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.1500
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
GATE_MODE=TRUE DIDT=TRUE

PPVIN_SW_LCDBKLT_SW
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V
SWITCH_MODE=TRUE DIDT=TRUE

PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1500
VOLTAGE=55V

BOM_COST_GROUP=DISPLAY

PAGE TITLE	LCD Backlight Driver
	Apple Inc.
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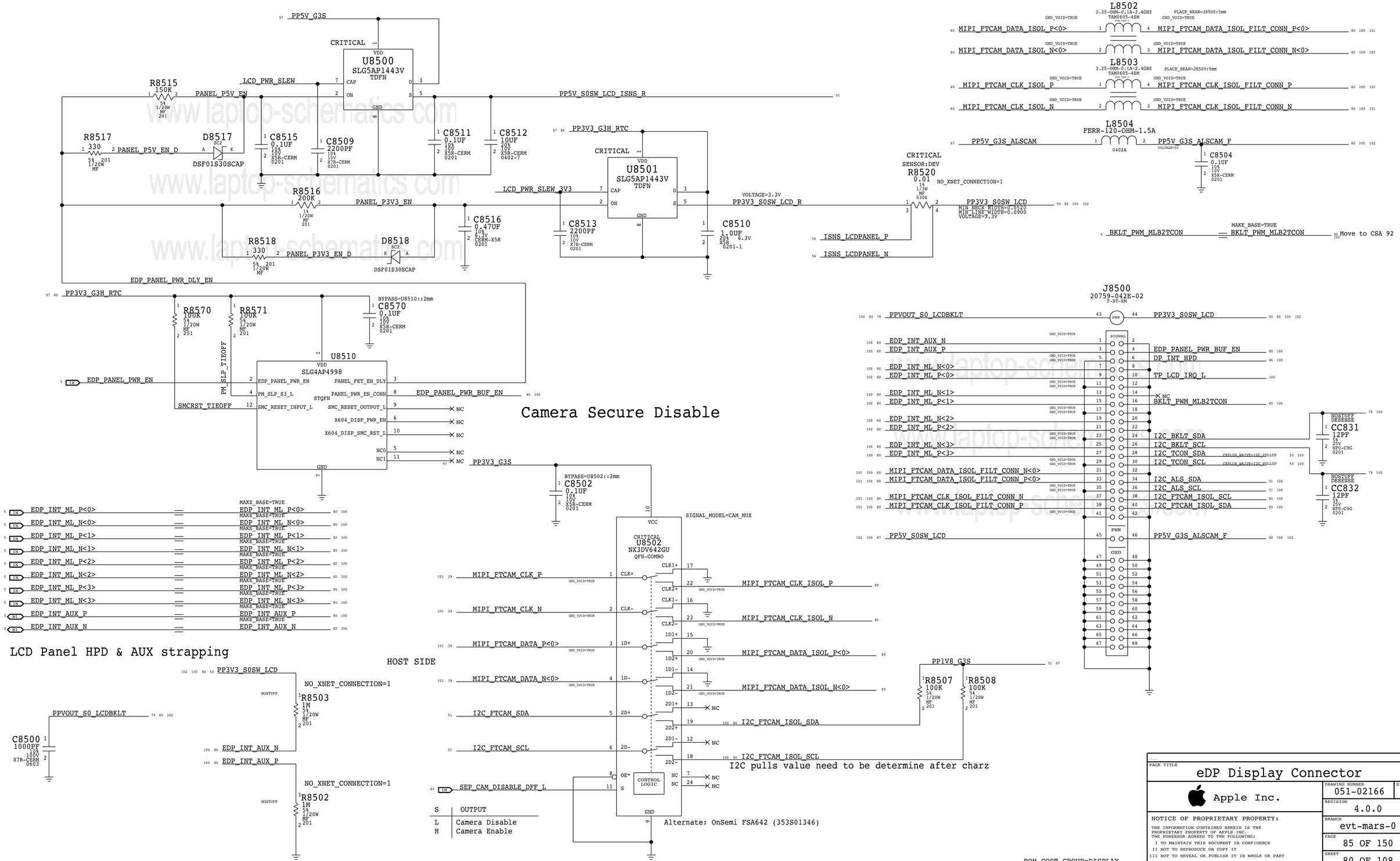
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



PAGE TITLE

eDP Display Connector

Apple Inc.

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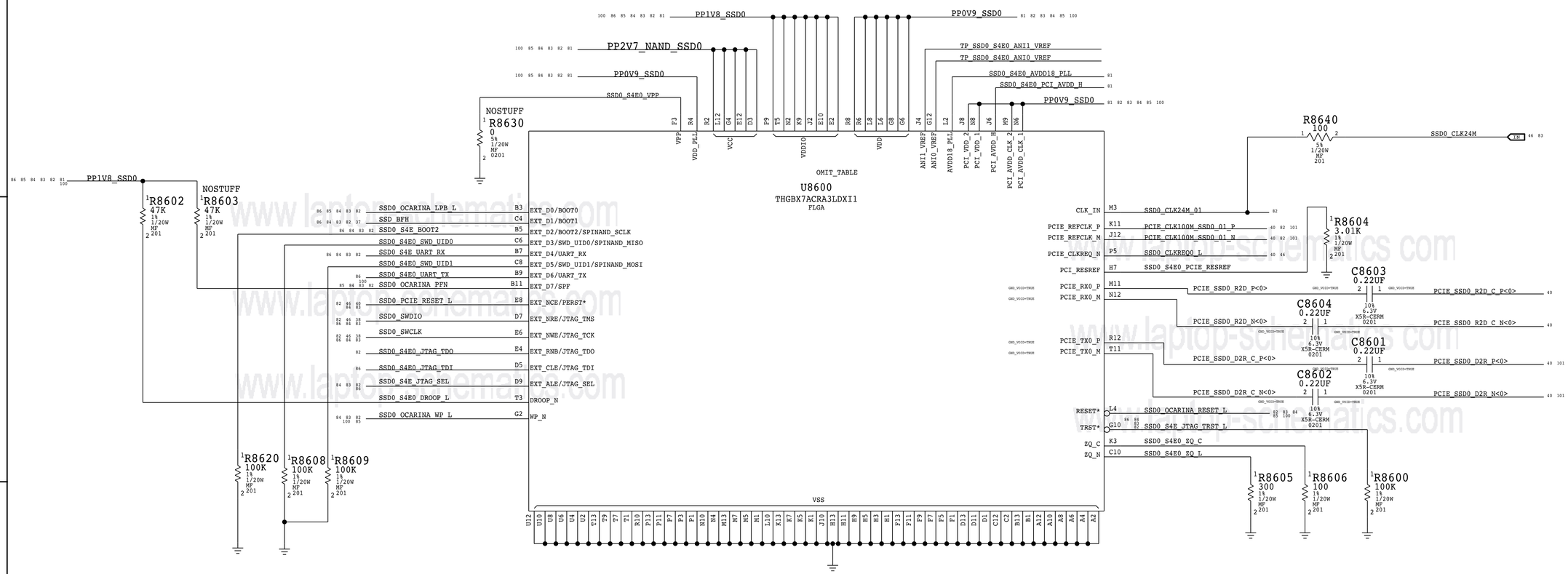
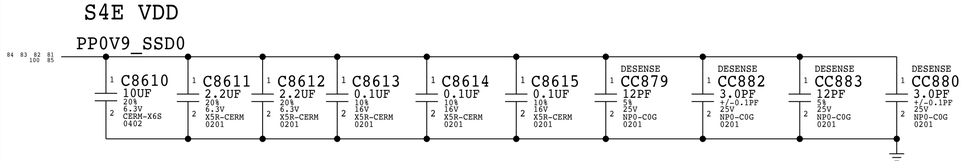
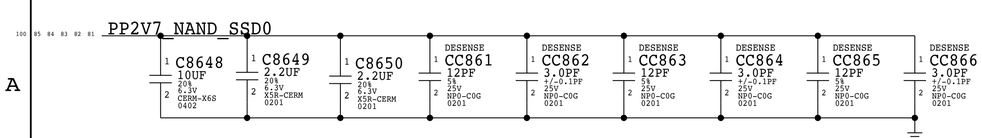
S4E0



S4E VDD



VCC CAP



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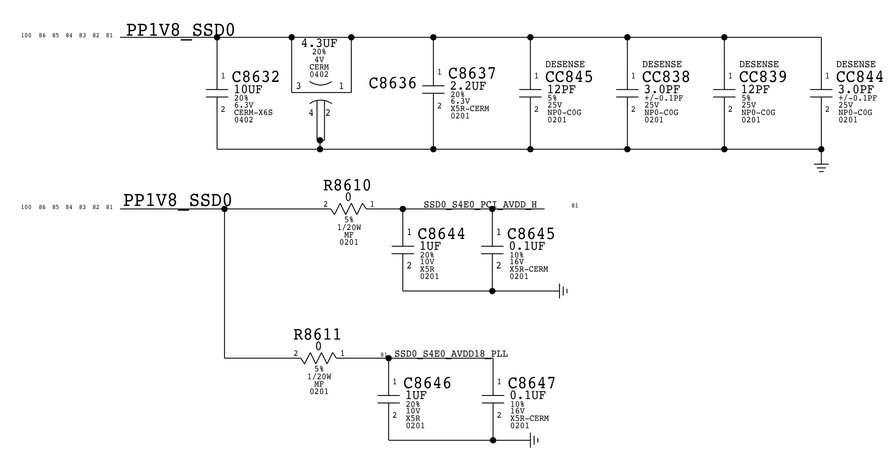

BOM_COST_GROUP=SSD

SYNC_MASTER=J137_GS5_REDHEAD	SYNC_DATE=02/17/2017
PAGE TITLE: S4E<0>	
Apple Inc.	DRAWING NUMBER: 051-02166 / SIZE: D
	REVISION: 4.0.0
	BRANCH: evt-mars-0
	PAGE: 86 OF 150
	SHEET: 81 OF 108

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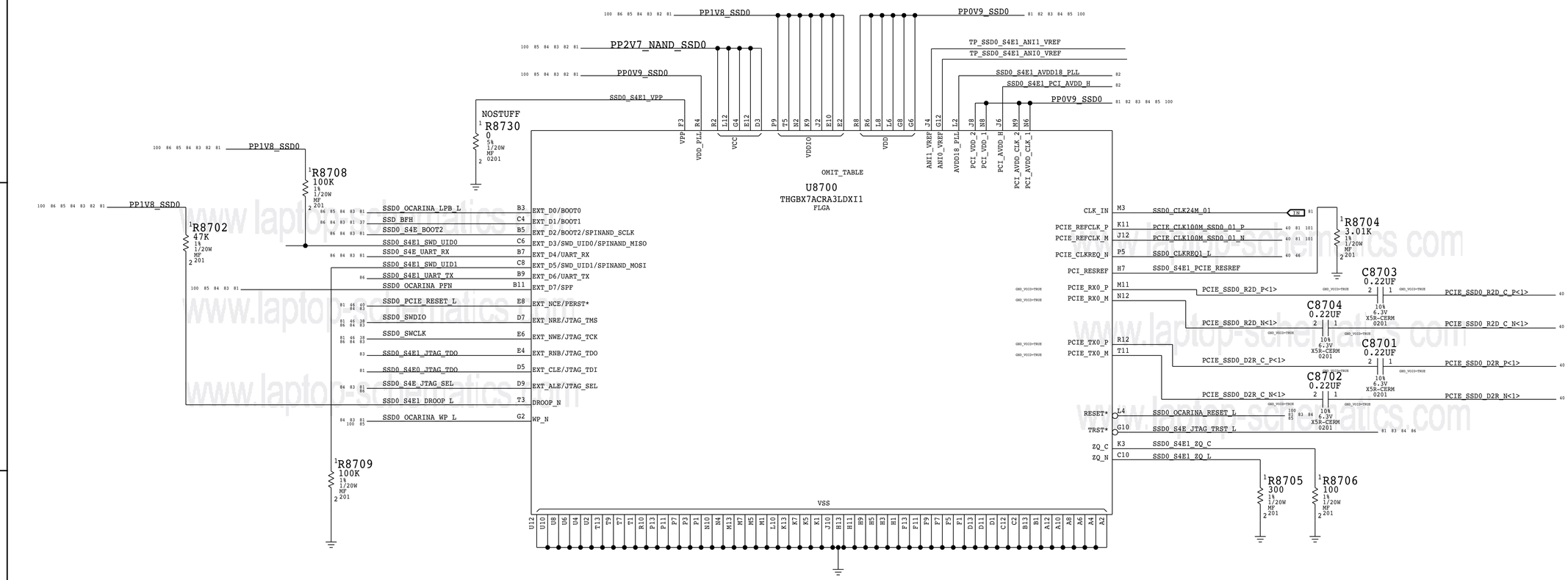
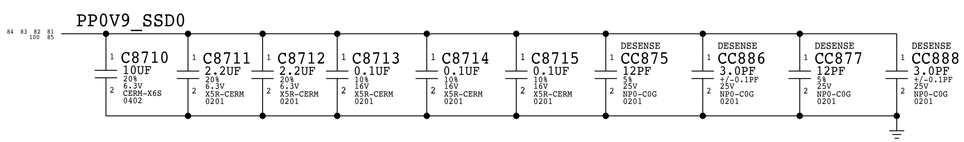
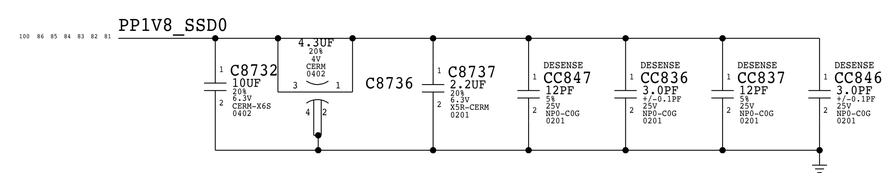
S4E1



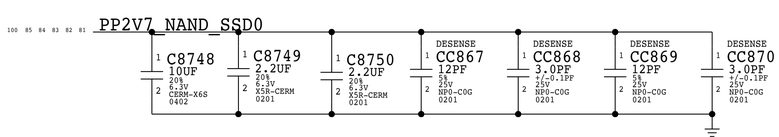
S4E VDD

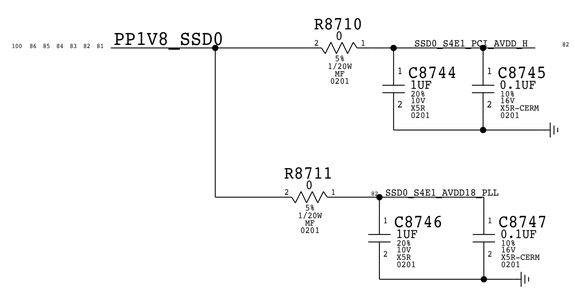


S4E VDDIO



VCC CAP





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SYNC_MASTER=J137_GS5_REDHEAD SYNC_DATE=02/17/2017

PAGE TITLE
S4E<1>

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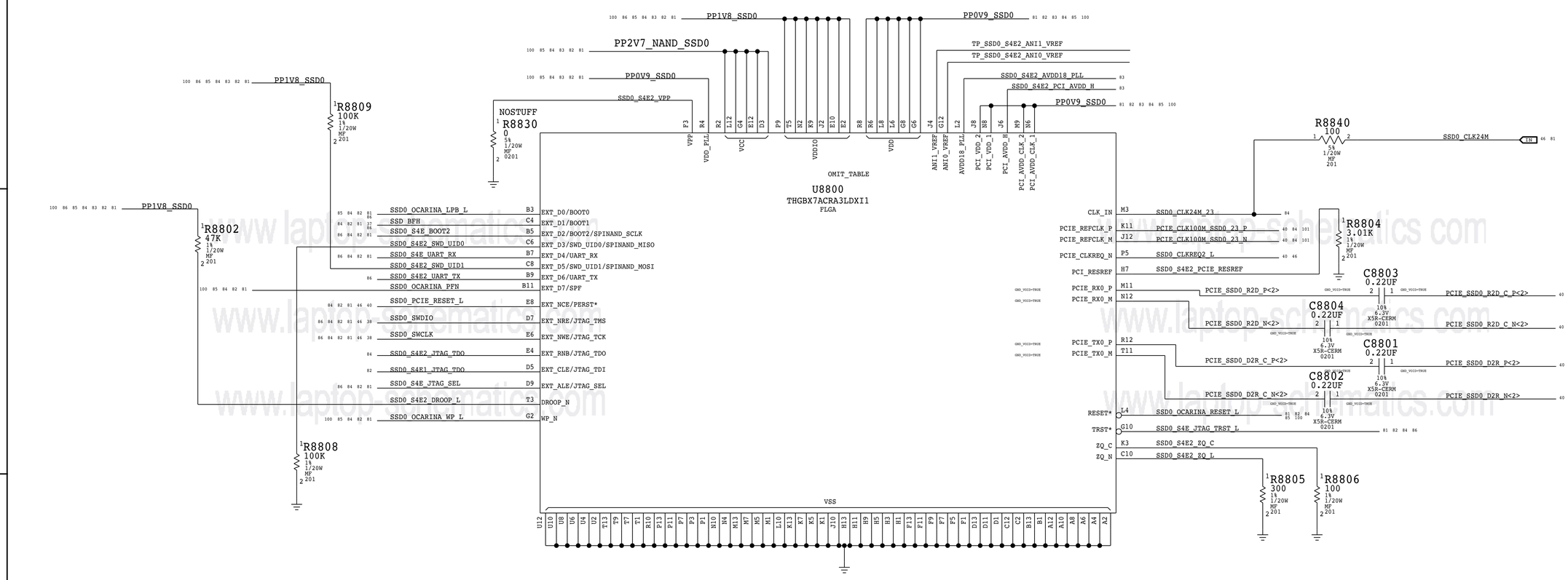
S4E2



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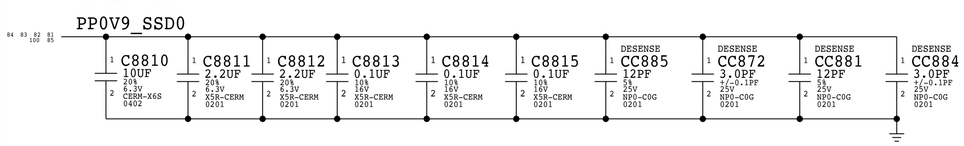

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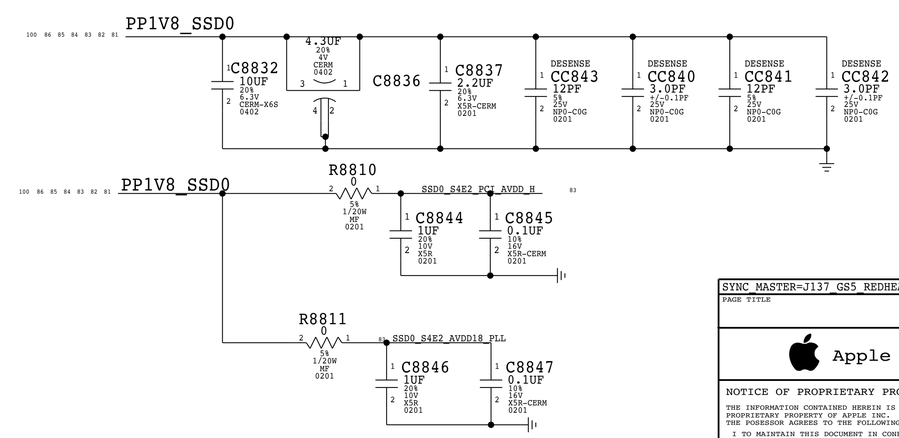

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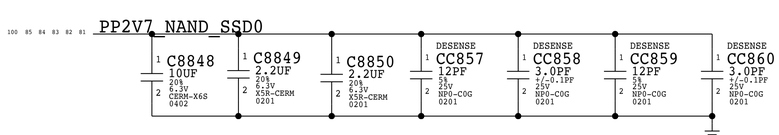

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SYNC_MASTER=J137_GS5_REDHEAD SYNC_DATE=02/17/2017

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DRAWING NUMBER: 051-02166 SIZE: D

REVISION: 4.0.0

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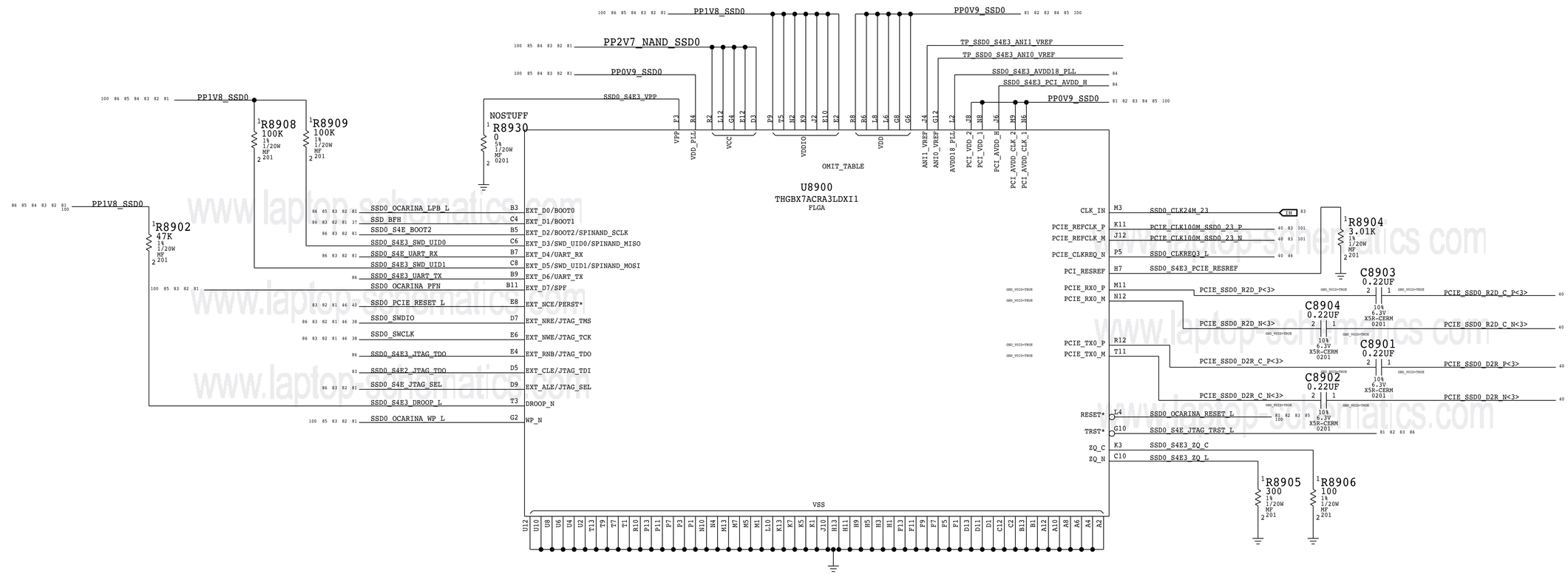
S4E3



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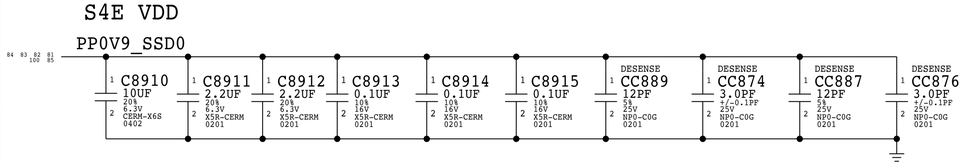

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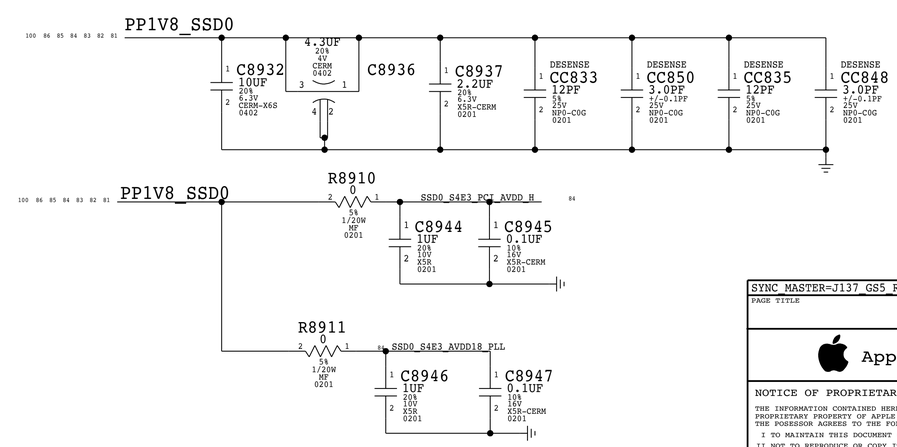

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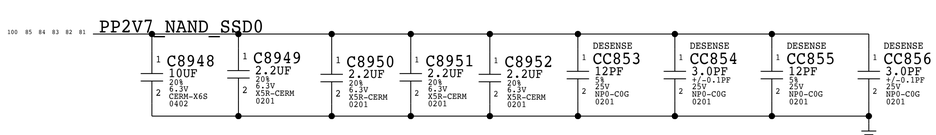

BOM_COST_GROUP=SSD

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SYNC_MASTER=J137_GS5_REDHEAD SYNC_DATE=02/17/2017

PAGE TITLE
S4E<3>

Apple Inc.

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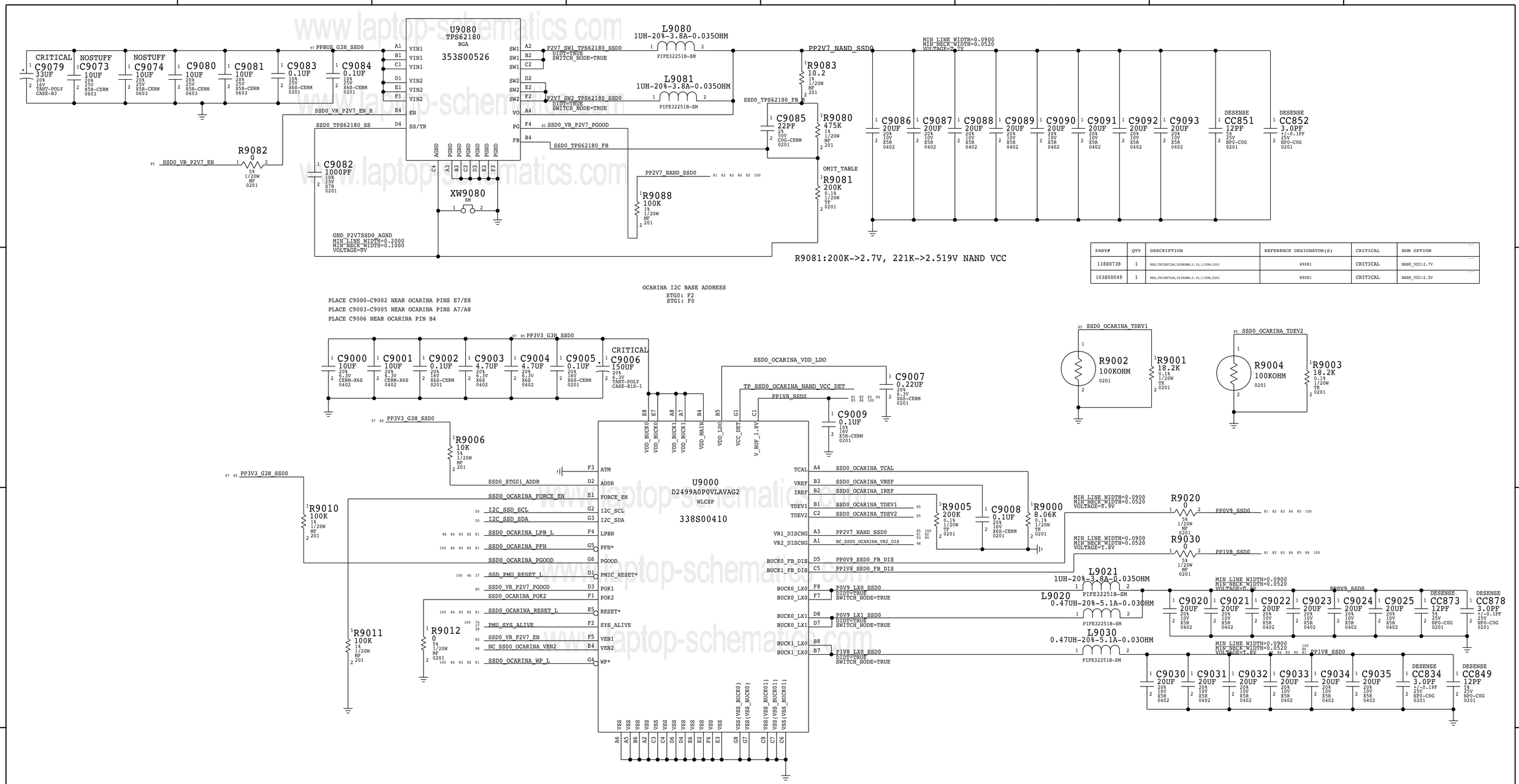

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0738	1	RES,THICKFILM,200KOHM,0.1%,1/20W,0201	R9081	CRITICAL	NAND_VCC:2.7V
103S00049	1	RES,THICKFILM,221KOHM,0.1%,1/20W,0201	R9081	CRITICAL	NAND_VCC:2.5V

SYNC_MASTER=J137_GS5_REDHEAD SYNC_DATE=02/17/2017

PAGE TITLE
OCARINA PMIC & NAND VCC VR

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REVISION 4.0.0
BRANCH evt-mars-0
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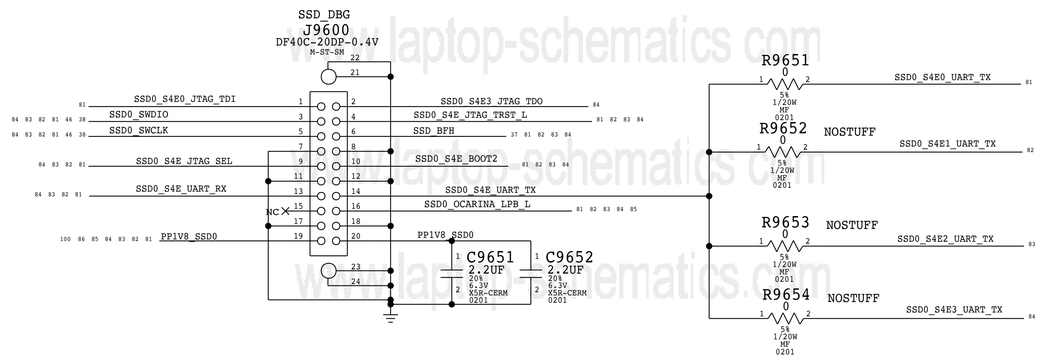
SSD0



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BOM_COST_GROUP=SSD

SYNC_MASTER=J680_MLB SYNC_DATE=03/20/2017

PAGE TITLE

SSD Support

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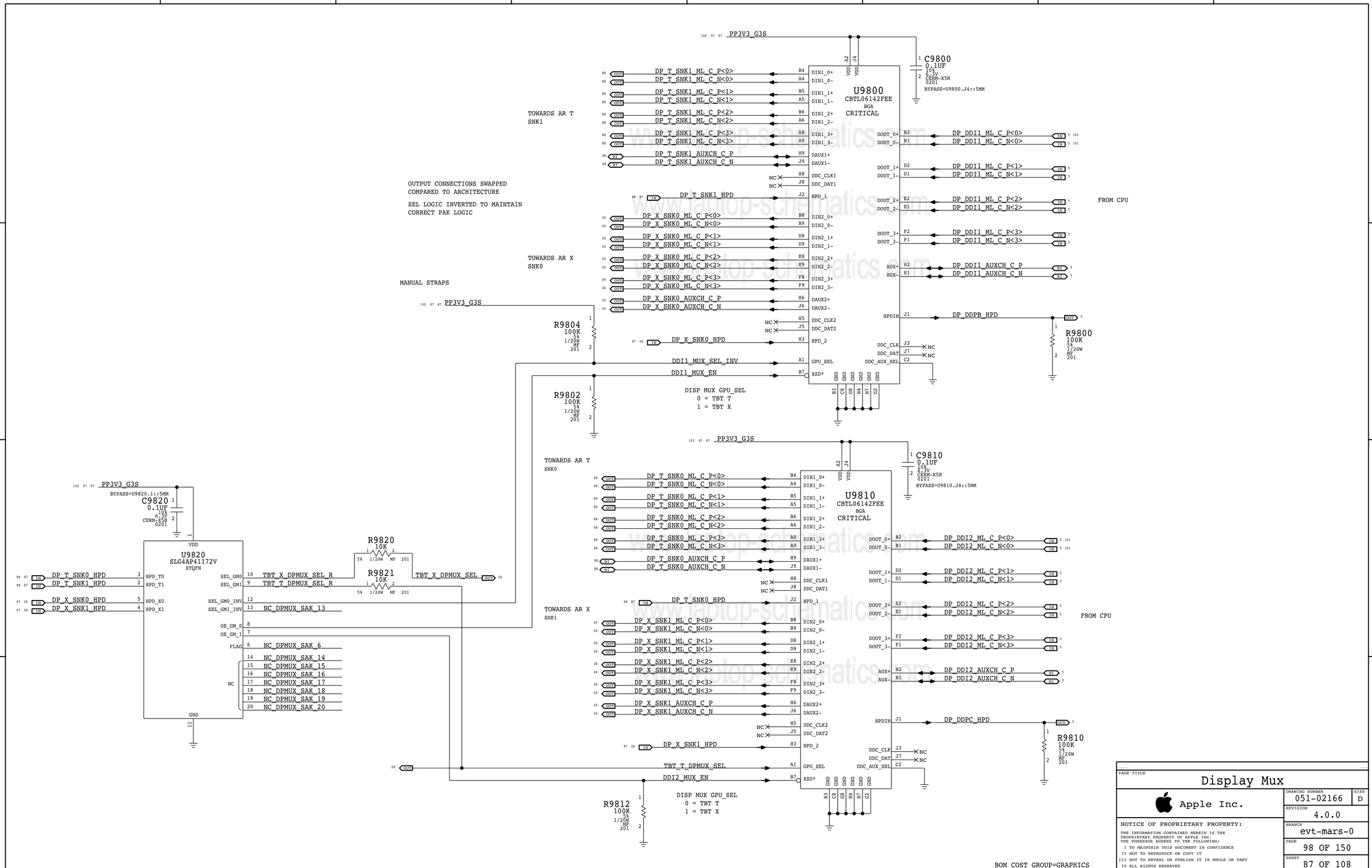
PP3V3_G3S
C9800
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=U9800.J4::5MM
U9800
CBTL06142FEE
BGA
CRITICAL
TOWARDS AR T
SNK1
DP_T_SNK1_ML_C_P<0>
DP_T_SNK1_ML_C_N<0>
DP_T_SNK1_ML_C_P<1>
DP_T_SNK1_ML_C_N<1>
DP_T_SNK1_ML_C_P<2>
DP_T_SNK1_ML_C_N<2>
DP_T_SNK1_ML_C_P<3>
DP_T_SNK1_ML_C_N<3>
DP_T_SNK1_AUXCH_C_P
DP_T_SNK1_AUXCH_C_N
DP_T_SNK1_HPD
OUTPUT CONNECTIONS SWAPPED
COMPARED TO ARCHITECTURE
SEL LOGIC INVERTED TO MAINTAIN
CORRECT PAK LOGIC
TOWARDS AR X
SNK0
DP_X_SNK0_ML_C_P<0>
DP_X_SNK0_ML_C_N<0>
DP_X_SNK0_ML_C_P<1>
DP_X_SNK0_ML_C_N<1>
DP_X_SNK0_ML_C_P<2>
DP_X_SNK0_ML_C_N<2>
DP_X_SNK0_ML_C_P<3>
DP_X_SNK0_ML_C_N<3>
DP_X_SNK0_AUXCH_C_P
DP_X_SNK0_AUXCH_C_N
DP_X_SNK0_HPD
MANUAL STRAPS
R9804
100K
5%
1/20W
MF
201
DDI1_MUX_SEL_INV
DDI1_MUX_EN
R9802
100K
5%
1/20W
MF
201
DISP MUX GPU_SEL
0 = TBT T
1 = TBT X
DP_DDI1_ML_C_P<0>
DP_DDI1_ML_C_N<0>
DP_DDI1_ML_C_P<1>
DP_DDI1_ML_C_N<1>
DP_DDI1_ML_C_P<2>
DP_DDI1_ML_C_N<2>
DP_DDI1_ML_C_P<3>
DP_DDI1_ML_C_N<3>
DP_DDI1_AUXCH_C_P
DP_DDI1_AUXCH_C_N
DP_DDPB_HPD
R9800
100K
5%
1/20W
MF
201
FROM CPU
C9810
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=U9810.J4::5MM
U9810
CBTL06142FEE
BGA
CRITICAL
TOWARDS AR T
SNK0
DP_T_SNK0_ML_C_P<0>
DP_T_SNK0_ML_C_N<0>
DP_T_SNK0_ML_C_P<1>
DP_T_SNK0_ML_C_N<1>
DP_T_SNK0_ML_C_P<2>
DP_T_SNK0_ML_C_N<2>
DP_T_SNK0_ML_C_P<3>
DP_T_SNK0_ML_C_N<3>
DP_T_SNK0_AUXCH_C_P
DP_T_SNK0_AUXCH_C_N
DP_T_SNK0_HPD
TOWARDS AR X
SNK1
DP_X_SNK1_ML_C_P<0>
DP_X_SNK1_ML_C_N<0>
DP_X_SNK1_ML_C_P<1>
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DP_X_SNK1_ML_C_N<3>
DP_X_SNK1_AUXCH_C_P
DP_X_SNK1_AUXCH_C_N
DP_X_SNK1_HPD
DP_DDI2_ML_C_P<0>
DP_DDI2_ML_C_N<0>
DP_DDI2_ML_C_P<1>
DP_DDI2_ML_C_N<1>
DP_DDI2_ML_C_P<2>
DP_DDI2_ML_C_N<2>
DP_DDI2_ML_C_P<3>
DP_DDI2_ML_C_N<3>
DP_DDI2_AUXCH_C_P
DP_DDI2_AUXCH_C_N
DP_DDPC_HPD
R9810
100K
5%
1/20W
MF
201
FROM CPU
C9820
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=U9820.1::5MM
U9820
SLG4AP41172V
STQFN
DP_T_SNK0_HPD
DP_T_SNK1_HPD
DP_X_SNK0_HPD
DP_X_SNK1_HPD
R9820
10K
5%
1/20W
MF
201
R9821
10K
5%
1/20W
MF
201
TBT_X_DPMUX_SEL_R
TBT_T_DPMUX_SEL_R
TBT_X_DPMUX_SEL
NC_DPMUX_SAK_13
NC_DPMUX_SAK_6
NC_DPMUX_SAK_14
NC_DPMUX_SAK_15
NC_DPMUX_SAK_16
NC_DPMUX_SAK_17
NC_DPMUX_SAK_18
NC_DPMUX_SAK_19
NC_DPMUX_SAK_20
TBT_T_DPMUX_SEL
DDI2_MUX_EN
R9812
100K
5%
1/20W
MF
201
DISP MUX GPU_SEL
0 = TBT T
1 = TBT X
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Display Mux
Apple Inc.
DRAWING NUMBER
051-02166
SIZE
D
REVISION
4.0.0
BRANCH
evt-mars-0
PAGE
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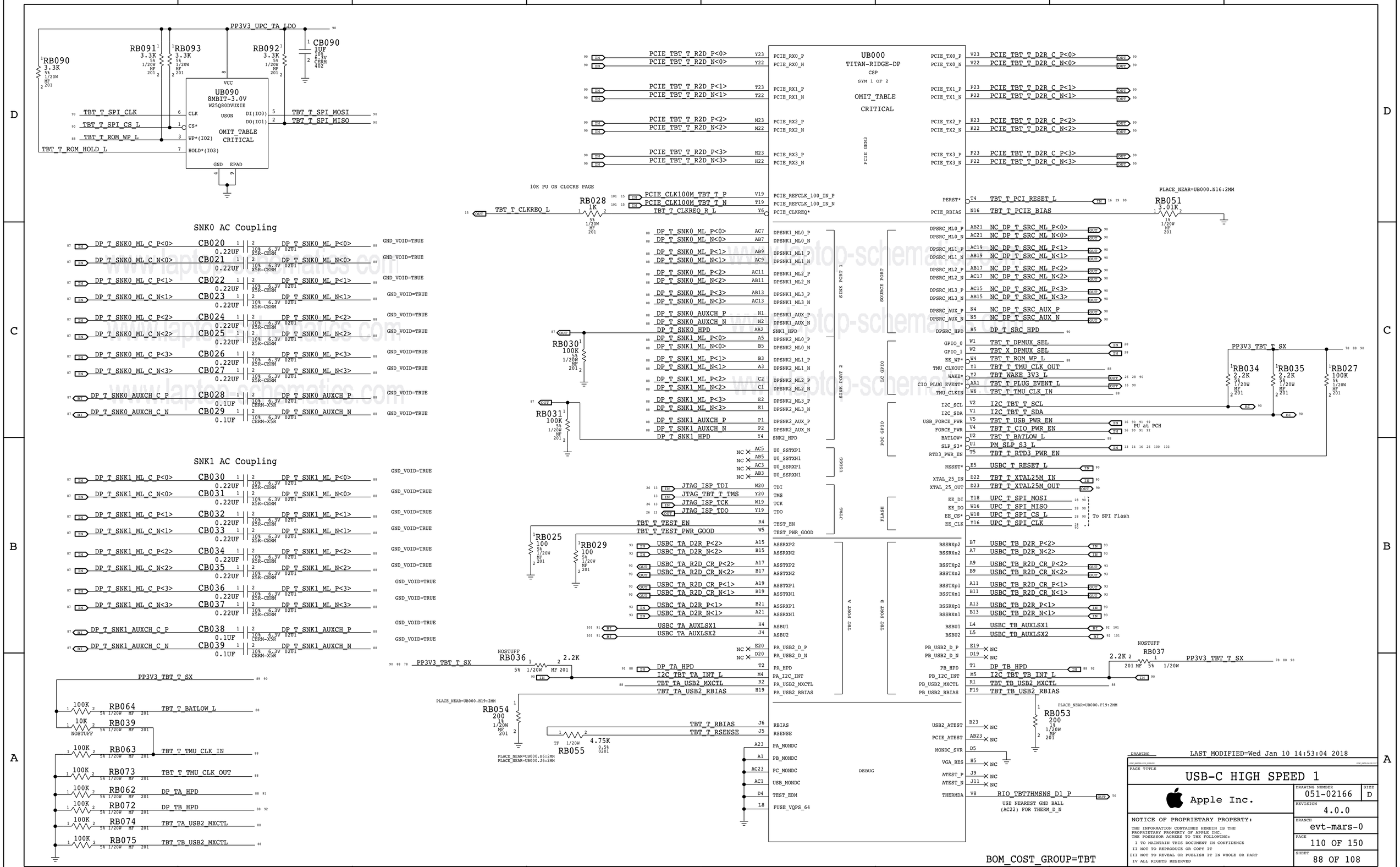
PP3V3_UPC_TA_LDO
RB090 3.3K
RB091 3.3K
RB093 3.3K
RB092 3.3K
CB090 1UF
UB090 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_ROM_WP_L
TBT_T_ROM_HOLD_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
UB000 TITAN-RIDGE-DP CSF SYM 1 OF 2
OMIT_TABLE CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
TBT_T_CLKREQ_L
RB028 1K
PLACE_NEAR=UB000.N16:2MM
RB051 3.01K
SINK PORT 1
SINK PORT 2
SOURCE PORT
LC GPIO
POC GPIO
FLASH
USB3S
JTAG
TBT PORT A
TBT PORT B
DEBUG
PU at PCH
To SPI Flash
RB030 100K
RB031 100K
RB025 100
RB029 100
RB036 2.2K
RB037 2.2K
RB054 200
RB053 200
RB055 4.75K
RB034 2.2K
RB035 2.2K
RB027 100K
RB064 100K
RB039 10K
RB063 100K
RB073 100K
RB062 100K
RB072 100K
RB074 100K
RB075 100K
USE NEAREST GND BALL (AC22) FOR THERM_D_N
BOM_COST_GROUP=TBT
LAST MODIFIED=Wed Jan 10 14:53:04 2018
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-02166
SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
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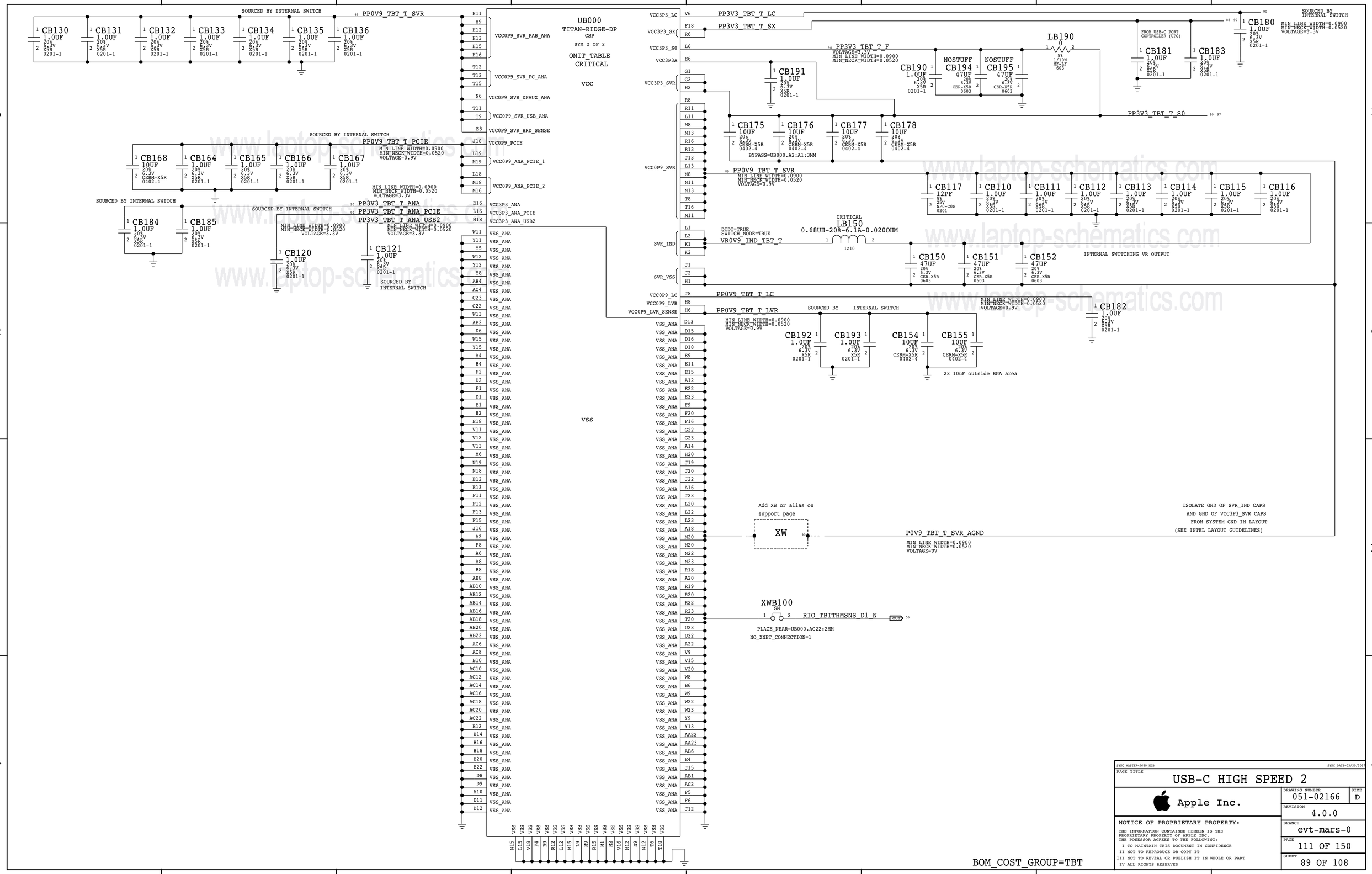

SYNC_MASTER=J680_MLB SYNC_DATE=03/30/2017

PAGE TITLE

USB-C HIGH SPEED 2

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Ridge 0.9V SVR XW

NO_XNET_CONNECTION=1
XWB200
SHORT-L6-SM

P0V9_TBT_T_SVR_AGND

DP SRC OPTIONS

IF DP SRC NOT USED

DP_T_SRC_HPD — RB240 100K 5% 1/20W MF 201

NC_DP_T_SRC_ML_P<0>	NC_DP_T_SRC_ML_P<0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_P<1>	NC_DP_T_SRC_ML_P<1>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_P<2>	NC_DP_T_SRC_ML_P<2>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_P<3>	NC_DP_T_SRC_ML_P<3>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<0>	NC_DP_T_SRC_ML_N<0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<1>	NC_DP_T_SRC_ML_N<1>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<2>	NC_DP_T_SRC_ML_N<2>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<3>	NC_DP_T_SRC_ML_N<3>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N	MAKE_BASE=TRUE NO_TEST=1

AR xtal

TBT_T_XTAL25M_OUT

CRITICAL
YB200
25MHZ-25PPM-20PF-50OHM
2.00X1.60-SM

CB202 20PF 5% 25V C0G 0201
CB203 20PF 5% 25V C0G 0201

TBT_T_XTAL25M_IN

ARKANOID DEBUG CONN

USBC_DBG — JB201 505070-1222 M-ST-SM — Place on bottom

TBT_T_PLUG_EVENT_L	1	TBT_T_PCI_RESET_L
TBT_WAKE_3V3_L	3	USBC_T_RESET_L
TBT_T_CIO_PWR_EN	5	PP3V3_TBT_T_SX
TBT_T_USB_PWR_EN	7	PP3V3_TBT_T_ANA_PCIE
TBT_POC_RESET	9	PP3V3_TBT_T_ANA
PP3V3_TBT_T_F	11	PP3V3_TBT_T_LC

ACE A/B RPD STRAPPING

USBC_TA_CC1	MAKE_BASE=TRUE	USBC_TA_CC1
USBC_TA_CC2	MAKE_BASE=TRUE	USBC_TA_CC2
USBC_TB_CC1	MAKE_BASE=TRUE	USBC_TB_CC1
USBC_TB_CC2	MAKE_BASE=TRUE	USBC_TB_CC2

ACE FET DCIN Bypass Caps

PPDCIN_G3H

CB211 0.1UF 10% 35V CER-X5R 0201
CB212 0.1UF 10% 35V CER-X5R 0201
CB213 0.1UF 10% 35V CER-X5R 0201
CB214 0.1UF 10% 35V CER-X5R 0201

ACE PDs

UPC_TA_DBG3	RB260	100K
UPC_TA_DBG4	RB261	100K
UPC_TB_DBG1	RB200	100K
UPC_TB_DBG2	RB201	100K
UPC_TB_DBG3	RB262	100K
UPC_TB_DBG4	RB263	100K
UPC_T_5V_EN	RB232	100K
TBT_TA_LSTX	RB235	1M
TBT_TA_LSRX	RB236	1M
TBT_TB_LSTX	RB237	1M
TBT_TB_LSRX	RB238	1M

ARKANOID DEBUG CONN

USBC_DBG — JB200 505070-1222 M-ST-SM — Place on bottom

I2C_TBT_TB_INT_L	1	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	3	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	5	I2C_TBT_T_SCL
UPC_I2C_INT_L	7	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	9	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	11	UPC_TA_UART_RX

T ACE-SMC I2C SERIES R'S

PLACE_NEAR=U3900:13mm
RB241 33 5% 1/20W MF 201

I2C_UPC_T_SDA2		I2C_UPC_SDA
I2C_UPC_T_SDA2	MAKE_BASE=TRUE	I2C_UPC_SDA
I2C_UPC_T_SDA2	CKPLUS_WAIVE=I2C_PULLUP	

PLACE_NEAR=U3900:13mm
RB242 33 5% 1/20W MF 201

I2C_UPC_T_SCL2		I2C_UPC_SCL
I2C_UPC_T_SCL2	MAKE_BASE=TRUE	I2C_UPC_SCL
I2C_UPC_T_SCL2	CKPLUS_WAIVE=I2C_PULLUP	

FUSES FOR UPC

FB200 0603 CRITICAL PLACE_NEAR=QB300:5MM
6AMP-32V-0.0095OHM
PP20V_USBC_TA_VBUS — PP20V_USBC_TA_VBUS_F

FB201 0603 CRITICAL PLACE_NEAR=QB400:5MM
6AMP-32V-0.0095OHM
PP20V_USBC_TB_VBUS — PP20V_USBC_TB_VBUS_F

GND ALIASES

GND

NC/NO TEST

NO_TEST=1
NC_UPC_TB_I2C_ADDR

NC_UPC_TA_SWD_CLK	MAKE_BASE=TRUE	NC_UPC_TA_SWD_CLK NO_TEST=1
NC_UPC_TA_SWD_DATA	MAKE_BASE=TRUE	NC_UPC_TA_SWD_DATA NO_TEST=1
NC_UPC_TA_GPIO7	MAKE_BASE=TRUE	NC_UPC_TA_GPIO7 NO_TEST=1
NC_UPC_TB_GPIO7		NC_UPC_TB_GPIO7

SIGNAL ALIASES

SMC_DEBUGPRT_TX	MAKE_BASE=TRUE	SMC_DEBUGPRT_TX
SMC_DEBUGPRT_RX	MAKE_BASE=TRUE	SMC_DEBUGPRT_RX
UPC_PMU_RESET	MAKE_BASE=TRUE	UPC_PMU_RESET
UPC_T_5V_EN	MAKE_BASE=TRUE	UPC_T_5V_EN
TBT_POC_RESET	MAKE_BASE=TRUE	TBT_POC_RESET
XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTD_OC_L
NC_USBC_TB_RESET_L	MAKE_BASE=TRUE	NC_USBC_TB_RESET_L
USBC_T_RESET_L	MAKE_BASE=TRUE	USBC_T_RESET_L
USB2_UPC_TA_N	MAKE_BASE=TRUE	USB2_UPC_TA_N
USB2_UPC_TA_P	MAKE_BASE=TRUE	USB2_UPC_TA_P
USB2_UPC_TB_N	MAKE_BASE=TRUE	USB2_UPC_TB_N
USB2_UPC_TB_P	MAKE_BASE=TRUE	USB2_UPC_TB_P
TP_UPC_TB_GPIO0	MAKE_BASE=TRUE	TP_UPC_TB_GPIO0
TP_UPC_TB_GPIO1	MAKE_BASE=TRUE	TP_UPC_TB_GPIO1

POWER ALIASES

PP3V3_UPC_TA_LDO	MAKE_BASE=TRUE	PP3V3_UPC_TA_LDO
PP20V_USBC_TA_VBUS	MAKE_BASE=TRUE	PP20V_USBC_TA_VBUS
PP20V_USBC_TB_VBUS	MAKE_BASE=TRUE	PP20V_USBC_TB_VBUS MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=5V
PP5V_S4_T_USBC	MAKE_BASE=TRUE	PP5V_S4_T_USBC
PP3V3_TBT_T_SX	MAKE_BASE=TRUE	PP3V3_TBT_T_SX MIN_LINE_WIDTH=0.1500 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_TBT_T_S0	MAKE_BASE=TRUE	PP3V3_TBT_T_S0 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=3.3V

PP1V8_SLPS2R — PP3V3_G3H

RB226 100K 201 MF 1/20W 5%

TBT_WAKE_L — TBT_WAKE_3V3_L

QB201
DMN2250UFB
DFN1006-3

TR/ACE SPI BUS SERIES R'S

TBT_T_SPI_CLK	RB290 100	TBT_T_SPI_CLK_DBG	
TBT_T_SPI_CLK	RB280 15	UPC_TA_SPI_CLK	Ace
TBT_T_SPI_CS_L	RB281 15	UPC_TA_SPI_CS_L	Ace
TBT_T_SPI_MOSI	RB282 15	UPC_TA_SPI_MOSI	Ace
TBT_T_SPI_MISO	RB283 15	UPC_TA_SPI_MISO	Ace
ROM	RB284 15	UPC_T_SPI_CLK	TR
	RB285 15	UPC_T_SPI_CS_L	TR
	RB286 15	UPC_T_SPI_MOSI	TR
	RB287 15	UPC_T_SPI_MISO	TR

TBT to ACE

TBT
Titan Ridge UB000
(MASTER)

Pri ACE
UB300
(Write: 0x70 Read: 0x71)

Sec ACE
UB400
(Write: 0x7E Read: 0x7F)

MAKE_BASE=TRUE	I2C_TBT_T_SCL	I2C_TBT_T_SCL
MAKE_BASE=TRUE	I2C_TBT_T_SDA	I2C_TBT_T_SDA
MAKE_BASE=TRUE	I2C_TBT_TA_INT_L	I2C_TBT_TA_INT_L
MAKE_BASE=TRUE	I2C_TBT_TB_INT_L	I2C_TBT_TB_INT_L
		I2C_TBT_T_SCL
		I2C_TBT_T_SDA
		I2C_TBT_TB_INT_L

Ridge PCIE Caps

D2R

PCIE_TBT_T_D2R_C_P<0>	CB250 0.22UF	PCIE_TBT_T_D2R_P<0>
PCIE_TBT_T_D2R_C_N<0>	CB251 0.22UF	PCIE_TBT_T_D2R_N<0>
PCIE_TBT_T_D2R_C_P<1>	CB252 0.22UF	PCIE_TBT_T_D2R_P<1>
PCIE_TBT_T_D2R_C_N<1>	CB253 0.22UF	PCIE_TBT_T_D2R_N<1>
PCIE_TBT_T_D2R_C_P<2>	CB254 0.22UF	PCIE_TBT_T_D2R_P<2>
PCIE_TBT_T_D2R_C_N<2>	CB255 0.22UF	PCIE_TBT_T_D2R_N<2>
PCIE_TBT_T_D2R_C_P<3>	CB256 0.22UF	PCIE_TBT_T_D2R_P<3>
PCIE_TBT_T_D2R_C_N<3>	CB257 0.22UF	PCIE_TBT_T_D2R_N<3>

R2D

PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF	PCIE_TBT_T_R2D_P<0>
PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF	PCIE_TBT_T_R2D_N<0>
PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF	PCIE_TBT_T_R2D_P<1>
PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF	PCIE_TBT_T_R2D_N<1>
PCIE_TBT_T_R2D_C_P<2>	CB244 0.22UF	PCIE_TBT_T_R2D_P<2>
PCIE_TBT_T_R2D_C_N<2>	CB245 0.22UF	PCIE_TBT_T_R2D_N<2>
PCIE_TBT_T_R2D_C_P<3>	CB246 0.22UF	PCIE_TBT_T_R2D_P<3>
PCIE_TBT_T_R2D_C_N<3>	CB247 0.22UF	PCIE_TBT_T_R2D_N<3>

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C Support

Apple Inc.

DRAWING NUMBER: 051-02166 SIZE: D
REVISION: 4.0.0
BRANCH: evt-mars-0
PAGE: 112 OF 150
SHEET: 90 OF 108

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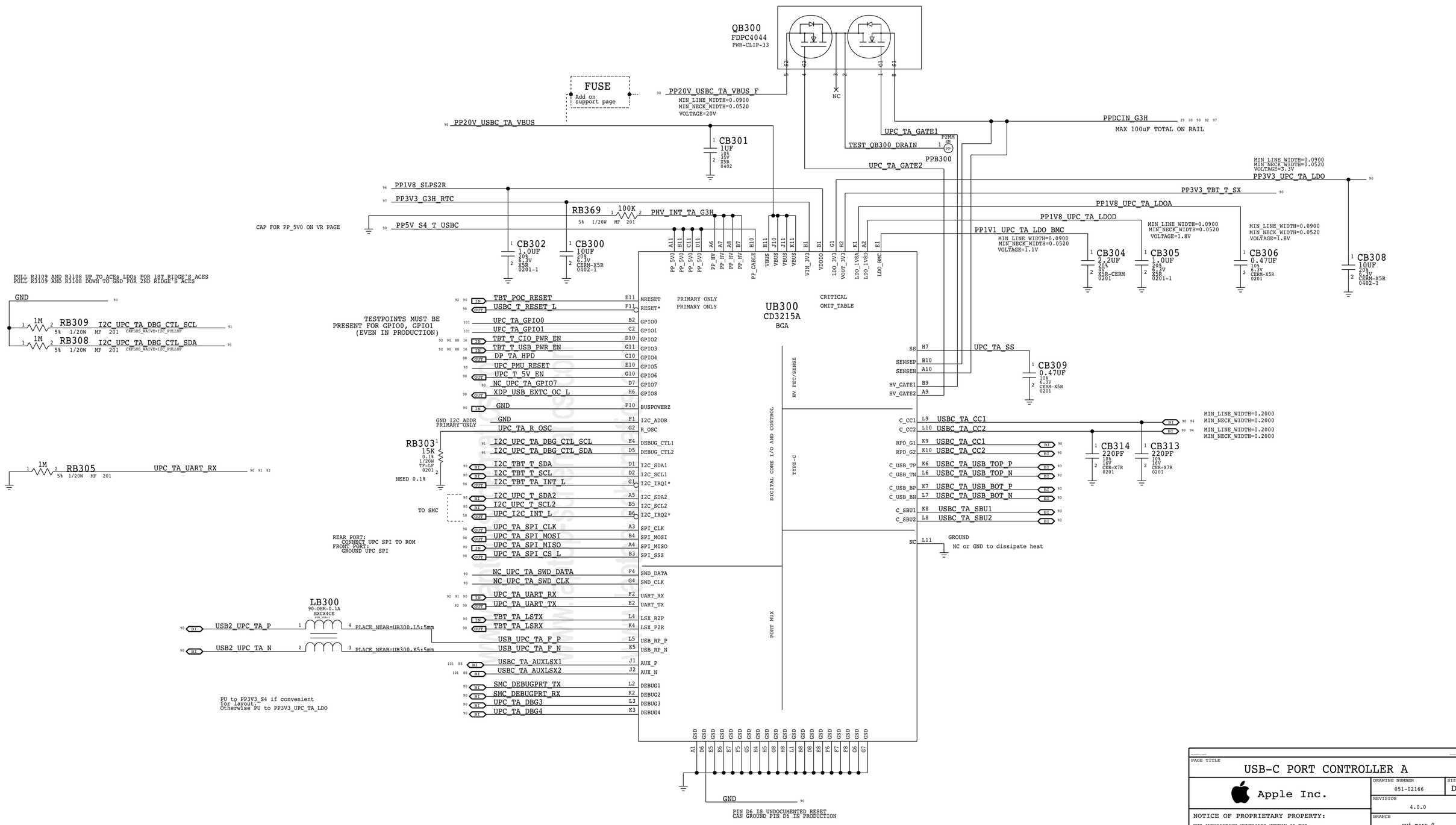
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER	051-02166
SIZE	D
REVISION	4.0.0
BRANCH	evt-mars-0
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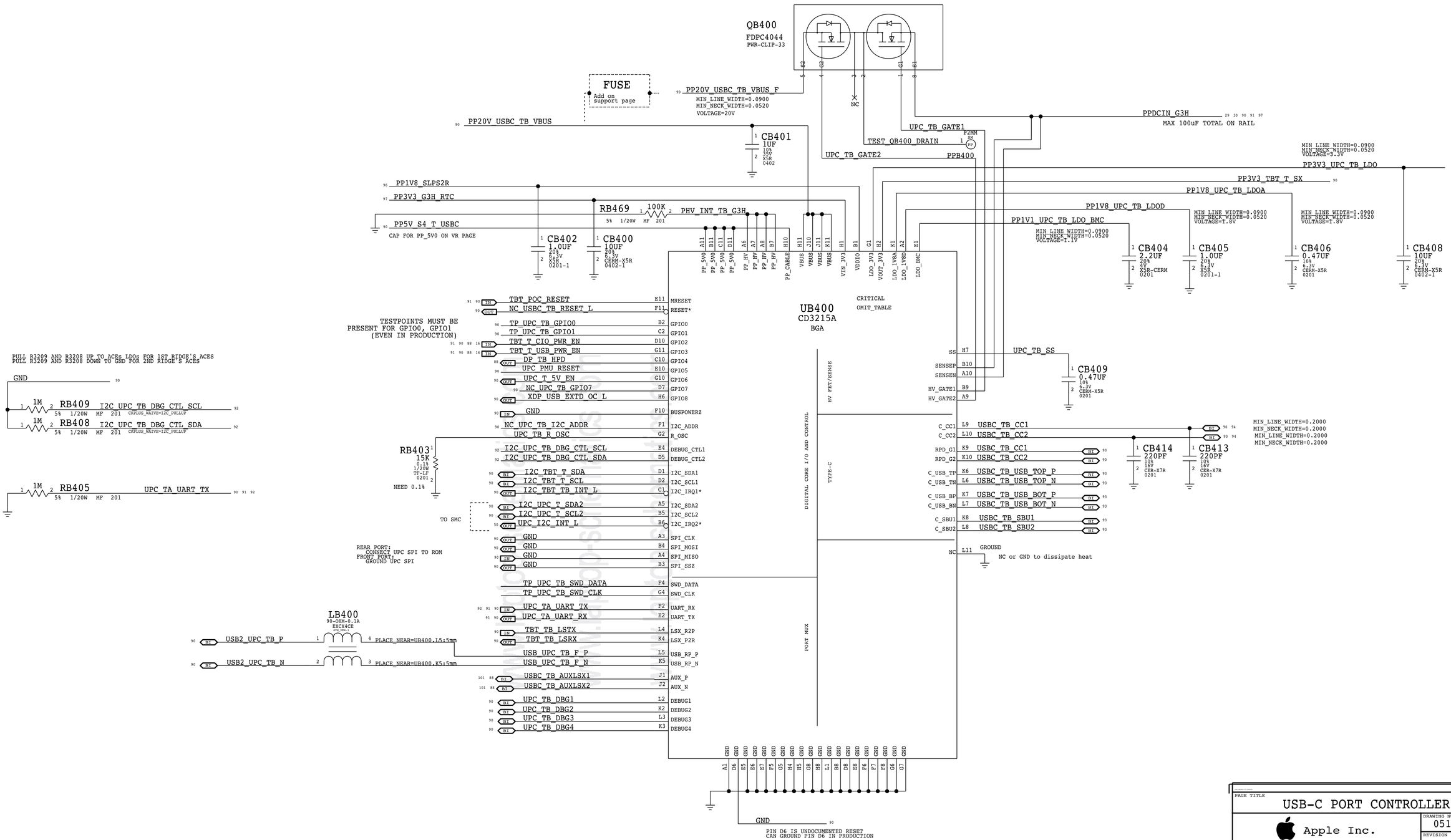
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER B

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DRAWING NUMBER 051-02166 SIZE D
REVISION 4.0.0
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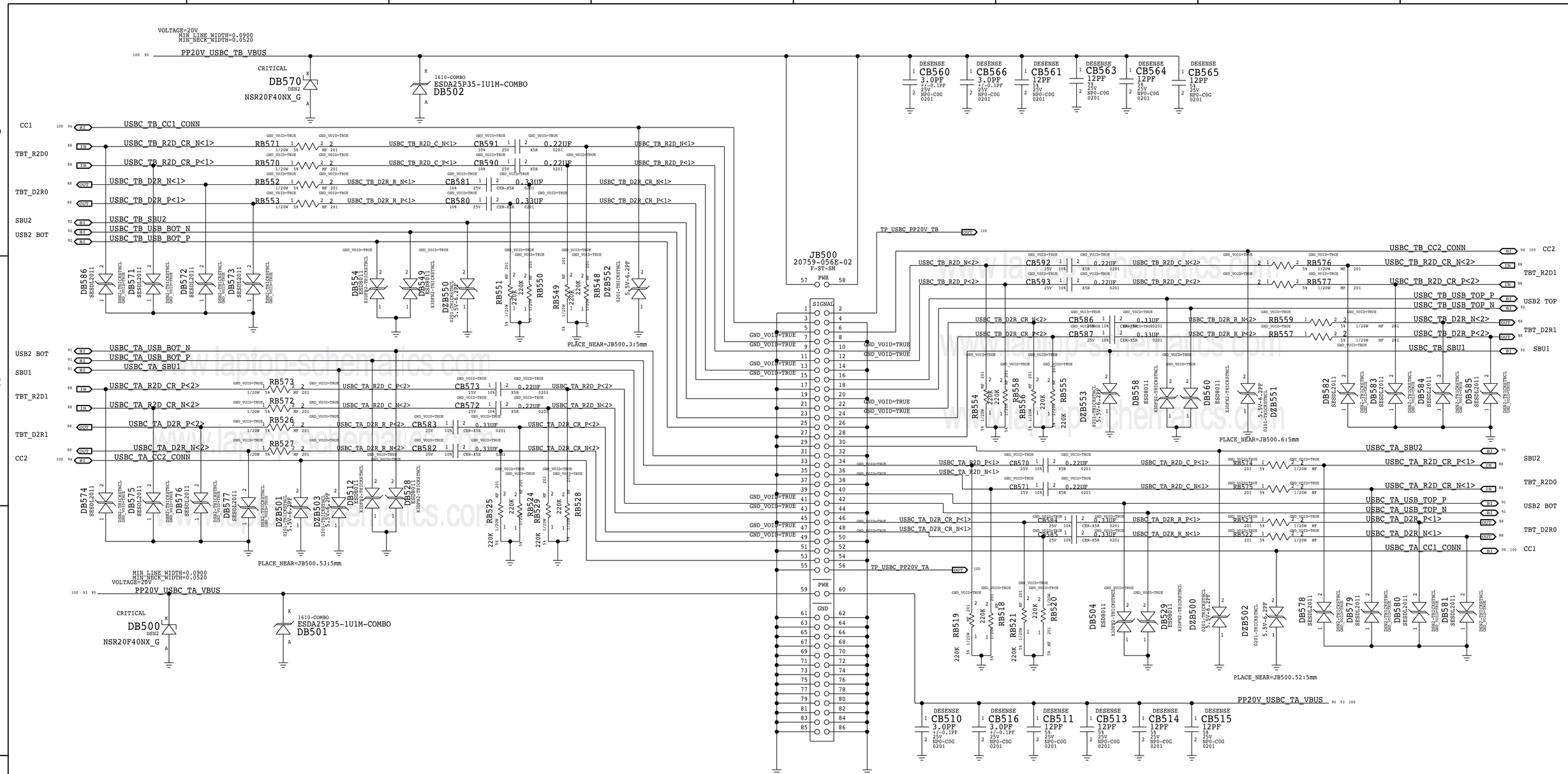

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BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-02166
SIZE D
REVISION 4.0.0
BRANCH evt-mars-0
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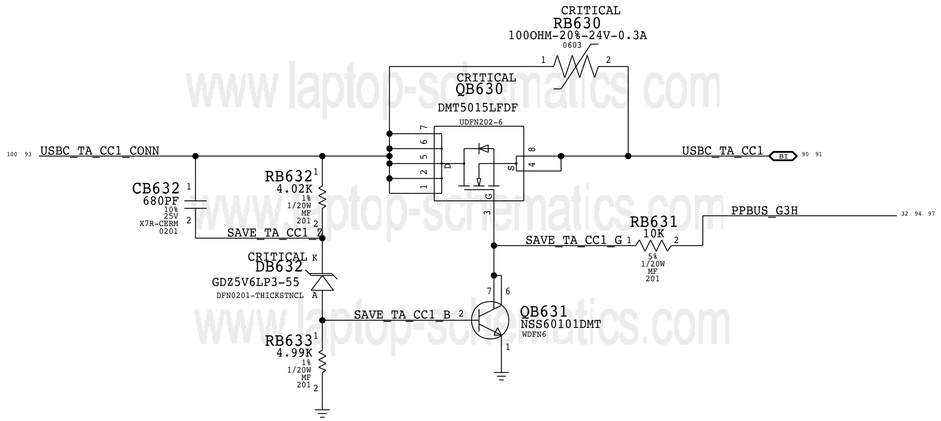
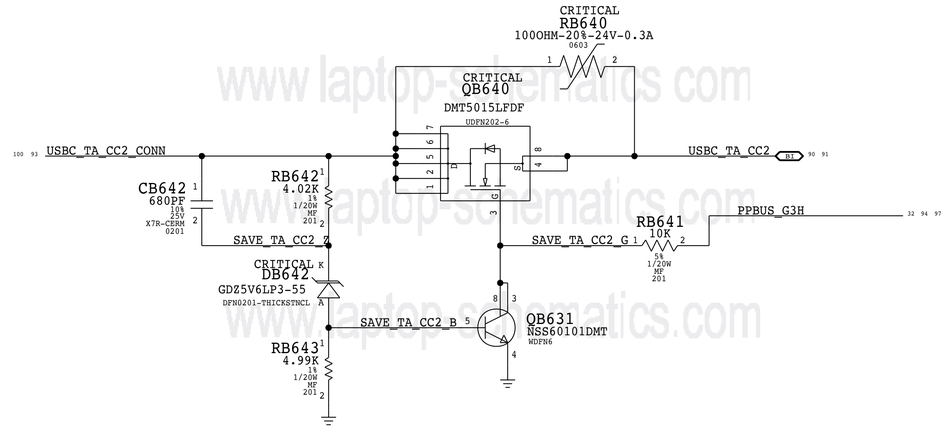
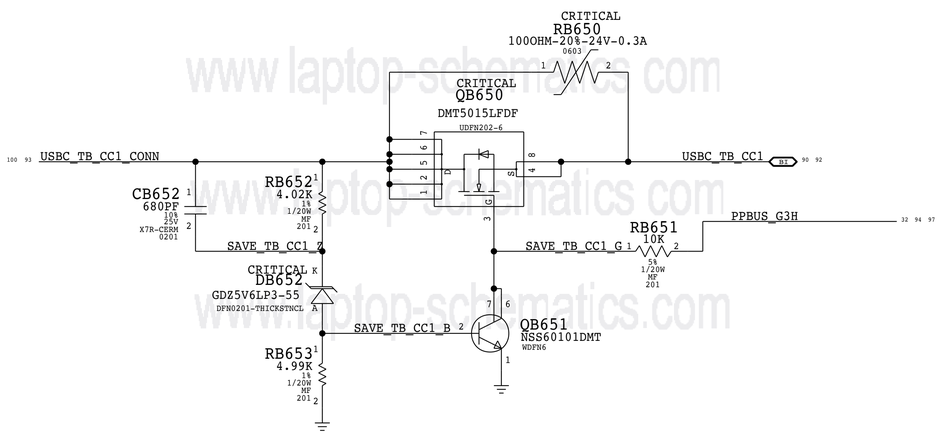
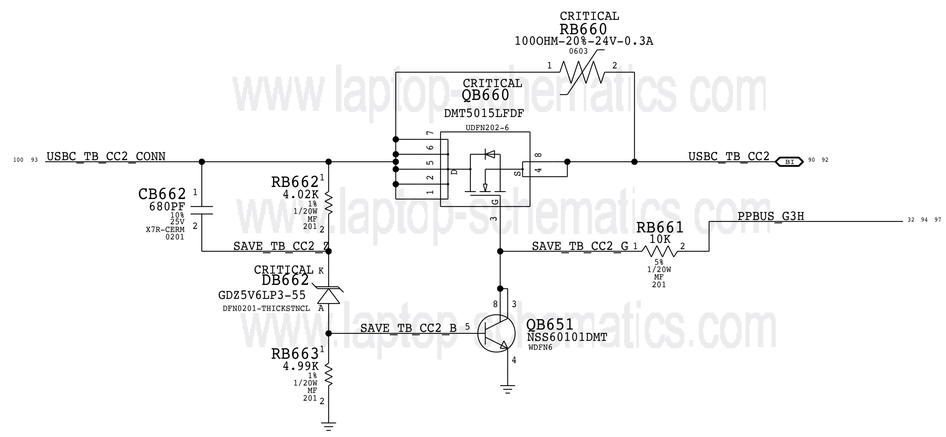
TA CC Protection





TB CC Protection





BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC T Connector Support

Apple Inc.

DRAWING NUMBER 051-02166
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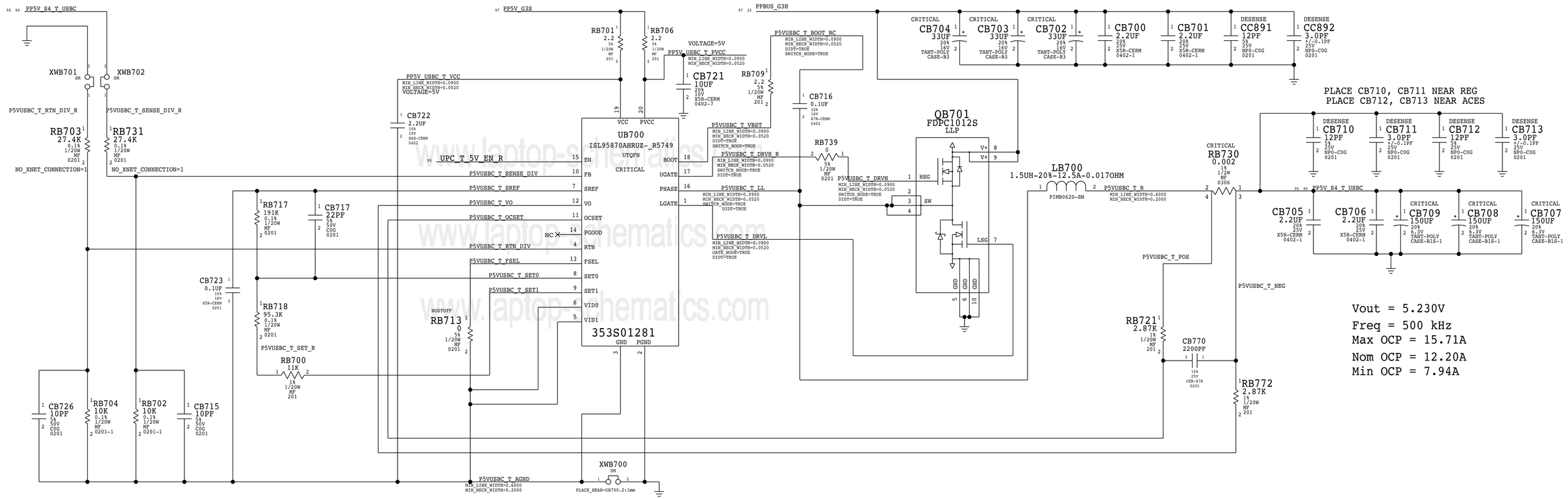
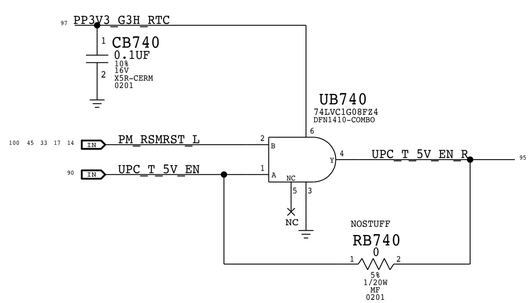


UPC T 5V EN QUALIFIER



BOM_COST_GROUP=USB-C

PAGE TITLE	TBT 5V REGULATOR
Apple Inc.	DRAWING NUMBER 051-02166 · SIZE D
	REVISION 4.0.0
	BRANCH evt-mars-0
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PMIC Buck0 - SoC VDD_CPU

PPVDDCPU_AWAKE (100 74)
Sourced from 3V3 G3H
Enabled by

- PPVDDCPU_AWAKE — MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.06V, MAKE_BASE=TRUE
- PPVDDCPU_AWAKE (41 46)

PMIC Buck1 - SoC VDD_CPU_SRAM

PPVDDCPUSRAM_AWAKE (100 74)
Sourced from 3V3 G3H
Enabled by

- PPVDDCPUSRAM_AWAKE — MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.06V, MAKE_BASE=TRUE
- PPVDDCPUSRAM_AWAKE (41)

PMIC Buck2 - SoC VDD_SOC

PP0V82_SLPDDR (100 74)
Sourced from 3V3 G3H
Enabled by

- PP0V82_SLPDDR — MIN_LINE_WIDTH=0.7000, MIN_NECK_WIDTH=0.0550, VOLTAGE=0.82V, MAKE_BASE=TRUE
- PP0V82_SLPDDR (41 46)

PMIC BUCK3 - SoC AOP/SMC/VDD1

PP1V8_SLPS2R (100 74 103)
Sourced from 3V3 G3H
Enabled by

- PP1V8_SLPS2R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_SLPS2R (74)
- PP1V8_SLPS2R (78)
- PP1V8_SLPS2R (75)
- PP1V8_SLPS2R (45)
- PP1V8_SLPS2R (76)
- PP1V8_SLPS2R (63)
- PP1V8_SLPS2R (45)
- PP1V8_SLPS2R (37 46 103)
- PP1V8_SLPS2R (43)
- PP1V8_SLPS2R (43)
- PP1V8_SLPS2R (43)
- PP1V8_SLPS2R (43)
- PP1V8_SLPS2R (90)
- PP1V8_SLPS2R (67)
- PP1V8_SLPS2R (50 66)
- PP1V8_SLPS2R (50)
- PP1V8_SLPS2R (50)
- PP1V8_SLPS2R (46)
- PP1V8_SLPS2R (29)
- PP1V8_SLPS2R (30)
- PP1V8_SLPS2R (91)
- PP1V8_SLPS2R (92)
- PP1V8_SLPS2R (103)

PMIC BUCK3 SW 1

PP1V8_AWAKE (100 74 103)
Sourced from PP1V8_SLPS2R
Enabled by

- PP1V8_AWAKE — MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_AWAKE (76)
- PP1V8_AWAKE (45)
- PP1V8_AWAKE (43)
- PP1V8_AWAKE (43)
- PP1V8_AWAKE (43)
- PP1V8_AWAKE (43)
- PP1V8_AWAKE (43)
- PP1V8_AWAKE (40 45 46)
- PP1V8_AWAKE (45)
- PP1V8_AWAKE (65)
- PP1V8_AWAKE (103)

PMIC BUCK3 SW 3

PP1V8_S5 (100 74)
Sourced from PP1V8_SLPS2R
Enabled by

- PP1V8_S5 — MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP1V8_S5 (8 12)
- PP1V8_S5 (13 14 15 16 38)
- PP1V8_S5 (12)
- PP1V8_S5 (19)
- PP1V8_S5 (19)
- PP1V8_S5 (35 76)
- PP1V8_S5 (8)
- PP1V8_S5 (19)
- PP1V8_S5 (50)
- PP1V8_S5 (50)
- PP1V8_S5 (45)
- PP1V8_S5 (68 73 77)
- PP1V8_S5 (78)
- PP1V8_S5 (73)
- PP1V8_S5 (77)
- PP1V8_S5 (103)
- PP1V8_S5 (56)
- PP1V8_S5 (56 102)
- PP1V8_S5 (50)
- PP1V8_S5 (45)
- PP1V8_S5 (17)
- PP1V8_S5 (19)
- PP1V8_S5 (45)

PMIC BUCK3 SW 4 - VDD1

PP1V8_S3 (100 74)
Sourced from PP1V8_SLPS2R
Enabled by

- PP1V8_S3 — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S3 (55)

PP1V8_S3_MEM (55)

- PP1V8_S3_MEM — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S3_MEM (21 22 23 24 100)

PMIC BUCK3 SW 5

NC_PP1V8_S0 (74)
Sourced from PP1V8_SLPS2R
Enabled by

- NC_PP1V8_S0 — MAKE_BASE=TRUE

PMIC Buck4 - SDRAM VDD2

PP1V1_SLPS2R (100 74)
Sourced from 3V3_G3H
Enabled by

- PP1V1_SLPS2R — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.1V, MAKE_BASE=TRUE
- PP1V1_SLPS2R (75)
- PP1V1_SLPS2R (75)
- PP1V1_SLPS2R (42)
- PP1V1_SLPS2R (43)

U7901 - VDDIO_DDR & PLL

PP1V1_SLPDDR (100 75)
Sourced from
Enabled by

- PP1V1_SLPDDR — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.1V, MAKE_BASE=TRUE
- PP1V1_SLPDDR (37)
- PP1V1_SLPDDR (42)
- PP1V1_SLPDDR (42)
- PP1V1_SLPDDR (43)

PMIC Buck5 - VDD_FIXED

PP0V9_SLPDDR (100 74)
Sourced from 3V3_G3H
Enabled by

- PP0V9_SLPDDR — MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.0550, VOLTAGE=0.9V, MAKE_BASE=TRUE
- PP0V9_SLPDDR (42)
- PP0V9_SLPDDR (42)
- PP0V9_SLPDDR (42)
- PP0V9_SLPDDR (42)
- PP0V9_SLPDDR (42)

PMIC Buck7 - VCCPRIM_CORE

PPVPCORE_S5 (100 74)
Sourced from 3V3_G3H
Enabled by

- PPVPCORE_S5 — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.05V, MAKE_BASE=TRUE
- PPVPCORE_S5 (8 12)

PMIC Buck8

PP1V_PRIM (100 74)
Sourced from 3V3_G3H
Enabled by

- PP1V_PRIM — MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.05V, MAKE_BASE=TRUE
- PP1V_PRIM (74)
- PP1V_PRIM (8 12)
- PP1V_PRIM (8)
- PP1V_PRIM (8)
- PP1V_PRIM (12)
- PP1V_PRIM (8)
- PP1V_PRIM (8)
- PP1V_PRIM (12)
- PP1V_PRIM (8)
- PP1V_PRIM (12)
- PP1V_PRIM (8 12)
- PP1V_PRIM (17)
- PP1V_PRIM (77)

PMIC Buck8 SW 2 - VCCPLL, VCCST

PP1V_S3 (100 74)
Sourced from PP1V05_PRIM
Enabled by

- PP1V_S3 — MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1.05V, MAKE_BASE=TRUE
- PP1V_S3 (8 10)
- PP1V_S3 (6 8 10 19)
- PP1V_S3 (73)
- PP1V_S3 (68)
- PP1V_S3 (76)
- PP1V_S3 (45)
- PP1V_S3 (45)

PMIC LDO0 - VDD_LOW

PP0V8_SLPS2R (100 75)
Sourced from PP1V1_SLP2R
Enabled by

- PP0V8_SLPS2R — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.06V, MAKE_BASE=TRUE
- PP0V8_SLPS2R (42)

PMIC LDO1 - PCH VCCRTC

PP3V_G3H_RTC (75)
Sourced from PP3V3_G3H
Enabled by

- PP3V_G3H_RTC — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0550, VOLTAGE=3V, MAKE_BASE=TRUE
- PP3V_G3H_RTC (8 12)
- PP3V_G3H_RTC (14 100)

PMIC LDO2 - PCIE_REFBUF/PLL

PP1V2_AWAKE (100 75)
Sourced from PP1V8_SLPS2R
Enabled by

- PP1V2_AWAKE — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0550, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_AWAKE (43)
- PP1V2_AWAKE (43)
- PP1V2_AWAKE (43)
- PP1V2_AWAKE (43)

PMIC HIO SW - VCCSTG

PP1V_S0SW (100 75)
Sourced from PP1V05_PRIM
Enabled by CPU_C10_GATE_L

- PP1V_S0SW — MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=1V, MAKE_BASE=TRUE
- PP1V_S0SW (6 8 10 17)

PMIC V3P3 SW 1 - USB

PP3V3_AWAKE (100 75)
Sourced from 3V3_G3H
Enabled by

- PP3V3_AWAKE — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0550, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_AWAKE (43)

PMIC V3P3 SW 2 -

PP3V3_S5 (100 75)
Sourced from 3V3_G3H
Enabled by

- PP3V3_S5 — MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S5 (8 12)
- PP3V3_S5 (45)
- PP3V3_S5 (5 13 14 15 19)
- PP3V3_S5 (50)
- PP3V3_S5 (8 12)
- PP3V3_S5 (19)
- PP3V3_S5 (19)
- PP3V3_S5 (78)
- PP3V3_S5 (73 77)
- PP3V3_S5 (8 13)
- PP3V3_S5 (103)
- PP3V3_S5 (103)

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Power Aliases - 1

Apple Inc.

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PBUS Rails

U7000 - PBUS

PPBUS_G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPBUS_HS_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2500
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPVIN_G3H_P5VG3S
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPVIN_G3H_P3V3G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPVIN_G3H_P3V3G3HRTC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPBUS_G3H_SSD0
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPBUS_G3H_SPKRAMP_LEFT
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPBUS_G3H_SPKRAMP_RIGHT
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V
MAKE_BASE=TRUE

5V Rails

U7600 - 5V G3S

PP5V_G3S

Sourced from PBus
Enabled by P5VG3S_EN

PP5V_G3S_CPUREG
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3S_TPAD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3S_KBD
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2500
VOLTAGE=5V
MAKE_BASE=TRUE

5V Rails Continued

PP5V_G3S_ALSCAM
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4SW
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4SW_ISNS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0SW_LCD_ISNS_R
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0SW_LCD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

U7550 - 5V LDO - UNUSED

PP5V_S5_LDO
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

3V3 Rails

U6960 - 3V3_G3H_RTC

PP3V3_G3H_RTC

Sourced from PBus
Enabled by CHGR_EN_MVR

PP3V3_G3H_RTC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_SSD0
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_RTC_MESA
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

U7660 - 3V3_G3H

PP3V3_G3H

Sourced from PBus
Enabled by PMU_VDDMAIN_EN

VOUT_RTC sourced from
PP3V3_G3H_RTC input to PMIC

PP3V3_G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_PMU_VDDMAIN
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_DFR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

U8250 - 3V3 Sensors

PP3V3_S4SW_SNS

Sourced from 3V3_G3H_RTC
Enabled by SENSOR_PWR_EN

PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3 Rails Continued

U8200 - 3V3_G3S

PP3V3_G3S

Sourced from 3V3_G3H_RTC
Enabled by P3V3G3S_EN

PP3V3_G3S
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

U8205 - 3V3_TBT_X_S0

PP3V3_S0_TBT_X_ISNS_R

Sourced from 3V3_G3H
Enabled by TBT_PWR_EN

PP3V3_S0_TBT_X_ISNS_R
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_TBT_X_S0

U8203 - 3V3_TBT_T_S0

PP3V3_S0_TBT_T_ISNS_R

Sourced from 3V3_G3H_RTC
Enabled by TBT_PWR_EN

PP3V3_S0_TBT_T_ISNS_R
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_TBT_T_S0

CPU/PCH Rails

U7100, U7210, U7220 (IMVP9) - VCCCORE

PPVCC_S0_CPU

Sourced from PBus
Enabled by CPU_VR_EN

PPVCC_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.5V
MAKE_BASE=TRUE

U7100, U7270 (IMVP9) - VCCSA

PPVCCSA_S0_CPU

PPVCCSA_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.5V
MAKE_BASE=TRUE

U7100, U7410, U7420, U7430 (IMVP9) - VCCGT

PPVCCGT_S0_CPU

PPVCCGT_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.5V
MAKE_BASE=TRUE

U7710 - VCCEDRAM

PPVCCEDRAM_S0_CPU

Sourced from PBus
Enabled by PM_OPC_ZVM_L
&& PVCCEDRAM_EN

PPVCCEDRAM_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1V
MAKE_BASE=TRUE

U8110 - VCCIO

PPVCCIO_S0_CPU

Sourced from PBus
Enabled by CPU_C10_GATE_L
&& PVCCIO_EN

PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.95V
MAKE_BASE=TRUE

U8207 - VCCPLL OC SW

PP1V2_S0SW

Sourced from PP1V2_S3
Enabled by CPU_C10_GATE_L
&& PVCCPLLOC_EN

PP1V2_S0SW
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.2V
MAKE_BASE=TRUE

Digital Ground

GND
VOLTAGE=0V
MIN_LINE_WIDTH=0.0600
MIN_NECK_WIDTH=0.0700

3V3 Rails Continued

PP3V3_G3S_WLANBT
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S_TPAD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S_KBD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

1V8 Rails

U8220 - 1V8_G3S

PP1V8_G3S

Sourced from 1V8 SLEEPS2R
Enabled by P1V8G3S_EN

PP1V8_G3S
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_G3S_WLANBT_VDDIO
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
MAKE_BASE=TRUE

Memory Rails

U8100 - Memory VDD2

PP1V2_S3

Sourced from PBUS
Enabled by PVDDQ_EN

PP1V2_S3
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3_CPUDDR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.6V
MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFDQ_A
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.6V
MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFCA_A
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.6V
MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFDQ_B
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.6V
MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFCA_A
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.6V
MAKE_BASE=TRUE

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Power Aliases - 2

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Unused SoC Signals

38	NC_ALTIMETER_INT	MAKE_BASE=TRUE	NO_TEST=1	NC_ALTIMETER_INT
38	NC_DISP_GCON_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_GCON_INT_L
39	NC_DFR_TOUCH_RSVD	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_RSVD
38	NC_ENET_LOW_PWR	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_LOW_PWR
38	NC_ENET_MEDIA_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_MEDIA_SENSE
40	NC_ENET_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_RESET_L
39	NC_FTCAM_CLK12M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_CLK12M_R
39	NC_FTCAM_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_RESET_L
37	NC_GNSS_DEV_WAKE	MAKE_BASE=TRUE	NO_TEST=1	NC_GNSS_DEV_WAKE
37	NC_GNSS_HOST_TIME	MAKE_BASE=TRUE	NO_TEST=1	NC_GNSS_HOST_TIME
39	NC_I2S_CODEC_MCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_CODEC_MCLK
39	NC_I2S_CODEC1_MCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_CODEC1_MCLK
39	NC_I2S_CODEC1_R2D_R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_CODEC1_R2D_R
39	NC_I2S_HAWKING_BCLK_R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_HAWKING_BCLK_R
39	NC_I2S_HAWKING_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_HAWKING_D2R
39	NC_I2S_HAWKING_LRCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_HAWKING_LRCLK
38	NC_MESA_MENUKEY_L	MAKE_BASE=TRUE	NO_TEST=1	NC_MESA_MENUKEY_L
38	NC_PCC_EVENT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCC_EVENT
15	NC_PCH_ENET_LOW_PWR	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_ENET_LOW_PWR
38	NC_SOC_PCH_GCON_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_PCH_GCON_INT_L
40	NC_PCIE_CLK100M_ENET_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENET_N
40	NC_PCIE_CLK100M_ENET_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENET_P
40	NC_PCIE_CLK100M_SSD1_01_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_SSD1_01_N
40	NC_PCIE_CLK100M_SSD1_01_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_SSD1_01_P
40	NC_PCIE_CLK100M_SSD1_23_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_SSD1_23_N
40	NC_PCIE_CLK100M_SSD1_23_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_SSD1_23_P
40	NC_PCIE_CLK100M_WLAN_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_WLAN_N
40	NC_PCIE_CLK100M_WLAN_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_WLAN_P
40	NC_PCIE_ENET_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2R_N
40	NC_PCIE_ENET_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2R_P
40	NC_PCIE_ENET_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2D_C_N
40	NC_PCIE_ENET_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2D_C_P
40	NC_PCIE_SSD1_D2R_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_SSD1_D2R_N<3..0>
40	NC_PCIE_SSD1_D2R_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_SSD1_D2R_P<3..0>
40	NC_PCIE_SSD1_R2D_C_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_SSD1_R2D_C_N<3..0>
40	NC_PCIE_SSD1_R2D_C_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_SSD1_R2D_C_P<3..0>
40	NC_PCIE_WLAN_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_D2R_N
40	NC_PCIE_WLAN_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_D2R_P
40	NC_PCIE_WLAN_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_R2D_C_N
40	NC_PCIE_WLAN_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_R2D_C_P
38	NC_PCIEDN_WAKE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN_WAKE_L
38	NC_PLCAM_PROX_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_PROX_INT_L
38	NC_PLCAM_ROMEO_B2B_DETECT	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_ROMEO_B2B_DETECT
39	NC_PLCAM_RX_CLK12M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_RX_CLK12M_R
39	NC_PLCAM_RX_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_RX_RESET_L
39	NC_PLCAM_TX_CLK12M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_CLK12M_R
39	NC_PLCAM_TX_INT	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_INT
39	NC_PLCAM_TX_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_RESET_L
37	NC_PLCAM_TX_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_THROTTLE
38	NC_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SDCONN_STATE_CHANGE_L
38	NC_SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_SELF_THROTTLE
38	NC_SMC_LED_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_LED_ONEWIRE
38	NC_SMC_TOPBLK_SWP_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_TOPBLK_SWP_L
38	NC_SPI_ALTIMETER_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_ALTIMETER_CS_L
38	NC_SPI_DESCRIPTOR_OVERRIDE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DESCRIPTOR_OVERRIDE_L
40	NC_SSD1_CLK24M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_CLK24M_R
40	NC_SSD1_CLKREQ0_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_CLKREQ0_L
40	NC_SSD1_CLKREQ1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_CLKREQ1_L
40	NC_SSD1_CLKREQ2_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_CLKREQ2_L
40	NC_SSD1_CLKREQ3_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_CLKREQ3_L
40	NC_SSD1_PCIE_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_PCIE_RESET_L
38	NC_SSD1_SWCLK_UART_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_SWCLK_UART_R2D
38	NC_SSD1_SWDIO_UART_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD1_SWDIO_UART_D2R
39	NC_PCHROM_SW_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCHROM_SW_EN
40	NC_PCIE_DN2_R2D_CP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN2_R2D_CP
40	NC_PCIE_DN2_R2D_CN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN2_R2D_CN
40	NC_PCIE_DN2_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN2_D2RP
40	NC_PCIE_DN2_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN2_D2RN
40	NC_PCIE_DN3_R2D_CP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_R2D_CP
40	NC_PCIE_DN3_R2D_CN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_R2D_CN
40	NC_PCIE_DN3_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_D2RP
40	NC_PCIE_DN3_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_D2RN
40	NC_PCIE_CLK100M_DN2P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_DN2P
40	NC_PCIE_CLK100M_DN2N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_DN2N
40	NC_PCIEDN2_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN2_CLKREQ_L
40	NC_PCIEDN2_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN2_RESET_L
40	NC_PCIE_CLK100M_DN3P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_DN3P
40	NC_PCIE_CLK100M_DN3N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_DN3N
40	NC_PCIEDN3_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN3_CLKREQ_L
40	NC_PCIEDN3_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN3_RESET_L
37	NC_SOC_USB_ID	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_USB_ID
41	NC_SOC_VDDSOC_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_VDDSOC_SENSE
41	NC_SOC_VSSCPU_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_VSSCPU_SENSE
41	NC_SOC_VSSSOC_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_VSSSOC_SENSE
38	NC_TPAD_VIBE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TPAD_VIBE_L
39	NC_UART_GNSS_D2R_CTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_GNSS_D2R_CTS_L
39	NC_UART_GNSS_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_GNSS_R2D_RTS_L
40	NC_WLAN_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_CLKREQ_L
37	NC_WLAN_DEV_WAKE	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_DEV_WAKE
40	NC_WLAN_PERST_L	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_PERST_L

TP SoC Signals

100 38	TP_SMC_FIXTURE_MODE_L	MAKE_BASE=TRUE		TP_SMC_FIXTURE_MODE_L
103 100 39	TP_SOC_DEBUGPRT_RX	MAKE_BASE=TRUE		TP_SOC_DEBUGPRT_RX
103 100 39	TP_SOC_DEBUGPRT_TX	MAKE_BASE=TRUE		TP_SOC_DEBUGPRT_TX
37	TEST_SOC_AMUXOUT	MAKE_BASE=TRUE		TEST_SOC_AMUXOUT 101
37	TEST_SOC_TST_CLKOUT	MAKE_BASE=TRUE		TEST_SOC_TST_CLKOUT 101

SoC Aliases

39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE
39	GND	MAKE_BASE=TRUE

Unused PMIC Signals

67	NC_CHGR_AUX_OK	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_AUX_OK
74	NC_GPU_THRMTRIP	MAKE_BASE=TRUE	NO_TEST=1	NC_GPU_THRMTRIP
74	NC_NAND_DISCHARGE_EN_HDD_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND_DISCHARGE_EN_HDD_PWR_EN
74	NC_NAND_RESET_L_SD_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND_RESET_L_SD_PWR_EN
74	NC_NAND_WP_L_ENET_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND_WP_L_ENET_PWR_EN
74	NC_PEARL_PWREN_P2V7NAND_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_PEARL_PWREN_P2V7NAND_EN
74	NC_PMU_CLK32K_GNSS_R	MAKE_BASE=TRUE	NO_TEST=1	NC_PMU_CLK32K_GNSS_R
74	NC_P3V3G3W_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_P3V3G3W_EN
74	NC_P3V3G3W_PGOOD	MAKE_BASE=TRUE	NO_TEST=1	NC_P3V3G3W_PGOOD
74	NC_PMU_CLK32K	MAKE_BASE=TRUE	NO_TEST=1	NC_PMU_CLK32K
74	NC_PPBUCK8_SW1	MAKE_BASE=TRUE	NO_TEST=1	NC_PPBUCK8_SW1

PMIC Aliases

74	PVCCEOPIO_EDRAM_PGOOD	MAKE_BASE=TRUE	PVCCEOPIO_EDRAM_PGOOD 73
74	GND	MAKE_BASE=TRUE	
74	GND	MAKE_BASE=TRUE	

Unused WIRELESS Signals

35	NC_I2S_BT_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_BT_D2R
35	NC_I2S_BT_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_BT_R2D
35	NC_WLAN_PMU_TEST	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_PMU_TEST

Unused SSD Signals

85	NC_SSD0_OCARINA_VEN2	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD0_OCARINA_VEN2
85	NC_SSD0_OCARINA_VR2_DIS	MAKE_BASE=TRUE	NO_TEST=1	NC_SSD0_OCARINA_VR2_DIS

SYNC_MASTER=J132_GAREN SYNC_DATE=04/12/2017

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Signal Aliases

Apple Inc.

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Memory Bit & Byte Swizzle

MAKE_BASE=TRUE

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SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=10/29/2013

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Apple Inc.

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Functional Test Points

J5110 - DFR Display Connector

100 49	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
49 39	IN	DFR_DISP_TE	FUNC_TEST=TRUE
49 37	IN	DFR_DISP_INT	FUNC_TEST=TRUE
49 39	IN	DFR_DISP_RESET_L	FUNC_TEST=TRUE
49	IN	PP3V3_G3HSW_DFR	FUNC_TEST=TRUE 3 TPs
101 49	IN	MIPI_DFR_CLK_FILT_CONN_P	FUNC_TEST=TRUE
101 49	IN	MIPI_DFR_CLK_FILT_CONN_N	FUNC_TEST=TRUE
101 49	IN	MIPI_DFR_DATA_FILT_CONN_P	FUNC_TEST=TRUE
101 49	IN	MIPI_DFR_DATA_FILT_CONN_N	FUNC_TEST=TRUE
102 100 51 49	IN	PP1V8_DFR	FUNC_TEST=TRUE 2 TPs
51 49	IN	I2C_DFR_SCL_R	FUNC_TEST=TRUE
51 49	IN	I2C_DFR_SDA_R	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		7 TPs	

J5100 - DFR Touch Connector

49	IN	DFR_TOUCH_LID_OPEN_L	FUNC_TEST=TRUE
49 39	IN	SPI_DFR_CS_L	FUNC_TEST=TRUE
49 46	IN	SPI_DFR_MOSI	FUNC_TEST=TRUE
51 49	IN	I2C_DFR_SCL_R	FUNC_TEST=TRUE
51 49	IN	I2C_DFR_SDA_R	FUNC_TEST=TRUE
49 39	IN	DFR_TOUCH_RESET_L	FUNC_TEST=TRUE
102 100 51 49	IN	PP1V8_DFR	FUNC_TEST=TRUE 2 TPs
49	IN	PP5V_G3S_DFR_FILT	FUNC_TEST=TRUE 1 TPs
100 49	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
49 46	IN	SPI_DFR_MISO_R	FUNC_TEST=TRUE
49 46	IN	SPI_DFR_CLK	FUNC_TEST=TRUE
49 46	IN	DFR_TOUCH_INT_L	FUNC_TEST=TRUE
49 39	IN	DFR_TOUCH_CLK32K_RESET_L	FUNC_TEST=TRUE
49	IN	TP_DFR_TOUCH_GPIO2	FUNC_TEST=TRUE
100 49	IN	TP_DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE
100 49	IN	TP_DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	

J6700 - Keyboard Connector

64	IN	PP5V_G3S_FAN_CONN	FUNC_TEST=TRUE 8 TPs
64	IN	GND_FAN	FUNC_TEST=TRUE 8 TPs
64 58	IN	FAN_LT_TACH	FUNC_TEST=TRUE
64 58	IN	FAN_LT_PWM	FUNC_TEST=TRUE
64 58	IN	FAN_RT_TACH	FUNC_TEST=TRUE
64 58	IN	FAN_RT_PWM	FUNC_TEST=TRUE
97 64	IN	PP5V_G3S_KBD	FUNC_TEST=TRUE 3 TPs
97 64	IN	PP3V3_G3H_RTC	FUNC_TEST=TRUE 1 TPs
100 64	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
97 64	IN	PP3V3_G3S_KBD	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
100 64	IN	I2C_KBD_SDA	FUNC_TEST=TRUE
100 64	IN	KBD_INT_L	FUNC_TEST=TRUE
100 64	IN	I2C_KBD_SCL	FUNC_TEST=TRUE
76 66 64	IN	PMU_RSLOC_RST_L	FUNC_TEST=TRUE
103 100 64	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	

J6701 - Trackpad Connector

100 64	IN	I2C_KBD_SCL	FUNC_TEST=TRUE
100 64	IN	I2C_KBD_SDA	FUNC_TEST=TRUE
100 64	IN	KBD_INT_L	FUNC_TEST=TRUE
65 64	IN	I2C_TPAD_3V3_SDA	FUNC_TEST=TRUE
65 64	IN	I2C_TPAD_3V3_SCL	FUNC_TEST=TRUE
97 64	IN	PP3V3_G3S_TPAD	FUNC_TEST=TRUE
64	IN	PP5V_G3S_TPAD_CONN	FUNC_TEST=TRUE
64	IN	ACT_GND	FUNC_TEST=TRUE
64	IN	PPVIN_S4_TPAD_FUSE	FUNC_TEST=TRUE
65 64	IN	SPI_TPAD_3V3_CLK	FUNC_TEST=TRUE
65 64	IN	TPAD_3V3_SPI_EN	FUNC_TEST=TRUE
65 64	IN	SPI_TPAD_3V3_MISO	FUNC_TEST=TRUE
65 64	IN	SPI_TPAD_3V3_CS_L	FUNC_TEST=TRUE
65 64	IN	SPI_TPAD_3V3_MOSI	FUNC_TEST=TRUE
65 64	IN	TPAD_3V3_SPI_INT_L	FUNC_TEST=TRUE
65 64	IN	TPAD_3V3_ACTUATOR_DISABLE_L	FUNC_TEST=TRUE
65 64 46	IN	TPAD_KBD_WAKE_L	FUNC_TEST=TRUE
64 49 46 100	IN	IPD_LID_OPEN	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
100 64	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	

J4900 - Mesa Connector

47	IN	PP3V0_MESA_FILT_CONN	FUNC_TEST=TRUE 2 TPs
	IN	SPI_MESA_MISO_CONN	FUNC_TEST=TRUE
47	IN	MESA_INT_CONN	FUNC_TEST=TRUE
47	IN	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE
47	IN	ESD_GND	FUNC_TEST=TRUE 1 TPs
47	IN	PP1V8_MESA_FILT_CONN	FUNC_TEST=TRUE 1 TPs
47	IN	SPI_MESA_MOSI_CONN	FUNC_TEST=TRUE
100 47	IN	PMU_ONOFF_R_L_CONN	FUNC_TEST=TRUE
47	IN	SPI_MESA_CLK_CONN	FUNC_TEST=TRUE
47	IN	PP16V0_MESA_FILT_CONN	FUNC_TEST=TRUE 1 TPs
		GND	FUNC_TEST=TRUE
		2 TPs	

J6640 - MIC Connector

63 46	IN	PDM_DMIC_CLK0	FUNC_TEST=TRUE
62	IN	AUD_DMIC0_DATA_CONN	FUNC_TEST=TRUE
	IN	PP1V8_DMIC	FUNC_TEST=TRUE 1 TPs
63 46	IN	PDM_DMIC_CLK1	FUNC_TEST=TRUE
62	IN	AUD_DMIC1_DATA_CONN	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	

J6400 - Left Tweeter Connector

61	IN	SPKRCONN_LT_OUTP	FUNC_TEST=TRUE
61	IN	SPKRCONN_LT_OUTN	FUNC_TEST=TRUE
61 39	IN	SPKR_ID0	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	

J6450 - Left Woofer Connector

61	IN	SPKRCONN_LW_OUTP	FUNC_TEST=TRUE
61	IN	SPKRCONN_LW_OUTN	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	

J6500 - Right Tweeter Connector

62	IN	SPKRCONN_RT_OUTP	FUNC_TEST=TRUE
62	IN	SPKRCONN_RT_OUTN	FUNC_TEST=TRUE
62 39	IN	SPKR_ID1	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	

J6550 - Right Woofer Connector

62	IN	SPKRCONN_RW_OUTP	FUNC_TEST=TRUE
62	IN	SPKRCONN_RW_OUTN	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	

J6600 - Audio Jack Connector

63	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE 4 TPs
63	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE 4 TPs
63	IN	AUD_CONN_RING2	FUNC_TEST=TRUE
	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
63	IN	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
63	IN	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
63	IN	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
63	IN	AUD_CONN_RING_SENSE	FUNC_TEST=TRUE
63	IN	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
63	IN	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		4 TPs	

J6950 - Battery Connector

100 67 66	IN	PPVBAT_G3H_CONN	FUNC_TEST=TRUE 8 TPs
		GND	FUNC_TEST=TRUE
		8 TPs	

J6951 - Battery Sense Connector

100 66	IN	SYS_DETECT_L	FUNC_TEST=TRUE
66	IN	SMBUS_3V3_BATT_SCL	FUNC_TEST=TRUE
66	IN	SMBUS_3V3_BATT_SDA	FUNC_TEST=TRUE
66 54	IN	BMON_IOUT	FUNC_TEST=TRUE
78 76 53 52	IN	SENSOR_PWR_EN	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		1 TPs	

J8500 - eDP Connector

100 80 79	IN	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
80	IN	I2C_FTCAM_ISOL_SCL	FUNC_TEST=TRUE
80	IN	I2C_FTCAM_ISOL_SDA	FUNC_TEST=TRUE
80 51	IN	I2C_ALS_SCL	FUNC_TEST=TRUE
80 51	IN	I2C_ALS_SDA	FUNC_TEST=TRUE
80 50	IN	I2C_TCON_SCL	FUNC_TEST=TRUE
80 50	IN	I2C_TCON_SDA	FUNC_TEST=TRUE
80 79	IN	I2C_BKLT_SCL	FUNC_TEST=TRUE
80 79	IN	I2C_BKLT_SDA	FUNC_TEST=TRUE
80	IN	BKLT_PWM_MLB2TCON	FUNC_TEST=TRUE
80	IN	TP_LCD_IRQ_L	FUNC_TEST=TRUE
80 46	IN	DP_INT_HPD	FUNC_TEST=TRUE
80	IN	EDP_PANEL_PWR_BUF_EN	FUNC_TEST=TRUE
102 100 80 50	IN	PP3V3_S0SW_LCD	FUNC_TEST=TRUE 7 TPs
102 100 97 80	IN	PP5V_S0SW_LCD	FUNC_TEST=TRUE 1 TPs
102 80	IN	PP5V_G3S_ALSCAM_F	FUNC_TEST=TRUE
101 80	IN	MIPI_FTCAM_CLK_ISOL_FILT_CONN_P	FUNC_TEST=TRUE
101 80	IN	MIPI_FTCAM_CLK_ISOL_FILT_CONN_N	FUNC_TEST=TRUE
101 80	IN	MIPI_FTCAM_DATA_ISOL_FILT_CONN_P<0>	FUNC_TEST=TRUE
101 80	IN	MIPI_FTCAM_DATA_ISOL_FILT_CONN_N<0>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<3>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<3>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<2>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<2>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<1>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<1>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<0>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<0>	FUNC_TEST=TRUE
80	IN	EDP_INT_AUX_P	FUNC_TEST=TRUE
80	IN	EDP_INT_AUX_N	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		8 TPs	

J3300 - Left USB-C Connector

100 31 28	IN	PP20V_USBC_XA_VBUS	FUNC_TEST=TRUE 4 TPs
		GND	FUNC_TEST=TRUE
		4 TPs	
	IN	USBC_XA_CC1_CONN	FUNC_TEST=TRUE
32 31	IN	USBC_XA_CC2_CONN	FUNC_TEST=TRUE
31 29	IN	USBC_XA_SBU1	FUNC_TEST=TRUE
31 29	IN	USBC_XA_SBU2	FUNC_TEST=TRUE
100 31 28	IN	PP20V_USBC_XB_VBUS	FUNC_TEST=TRUE 4 TPs
		GND	FUNC_TEST=TRUE
		4 TPs	
32 31	IN	USBC_XB_CC1_CONN	FUNC_TEST=TRUE
32 31	IN	USBC_XB_CC2_CONN	FUNC_TEST=TRUE
31	IN	TP_USBC_PP20V_XA	FUNC_TEST=TRUE
31	IN	TP_USBC_PP20V_XB	FUNC_TEST=TRUE

JB500 - Right USB-C Connector

100 93 90	IN	PP20V_USBC_TA_VBUS	FUNC_TEST=TRUE 4 TPs
		GND	FUNC_TEST=TRUE
		4 TPs	
94 93	IN	USBC_TA_CC1_CONN	FUNC_TEST=TRUE
94 93	IN	USBC_TA_CC2_CONN	FUNC_TEST=TRUE
100 93 90	IN	PP20V_USBC_TB_VBUS	FUNC_TEST=TRUE 4 TPs
		GND	FUNC_TEST=TRUE
		4 TPs	
94 93	IN	USBC_TB_CC1_CONN	FUNC_TEST=TRUE
94 93	IN	USBC_TB_CC2_CONN	FUNC_TEST=TRUE
93	IN	TP_USBC_PP20V_TB	FUNC_TEST=TRUE
93	IN	TP_USBC_PP20V_TA	FUNC_TEST=TRUE

Probe Block Grid - DFU/SOC

15	IN	TP_USB_FIXT1_N	FUNC_TEST=TRUE
15	IN	TP_USB_FIXT1_P	FUNC_TEST=TRUE
15	IN	TP_USB_FIXT2_N	FUNC_TEST=TRUE
15	IN	TP_USB_FIXT2_P	FUNC_TEST=TRUE
15	IN	TP_USB3_EXTC_D2R_N	FUNC_TEST=TRUE
15	IN	TP_USB3_EXTC_D2R_P	FUNC_TEST=TRUE
15	IN	TP_USB3_EXTC_R2D_C_N	FUNC_TEST=TRUE
15	IN	TP_USB3_EXTC_R2D_C_P	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		3 TPs; 1x for USB2 pair, 1x for USB3 R2D, 1x for USB3 D2R	
100 97 67	IN	PPDCIN_G3H	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	

DFU/SOC/FCT DEBUG

103 37 28	IN	SOC_USB_VBUS	FUNC_TEST=TRUE
103 76 37 28	IN	SOC_FORCE_DFU	FUNC_TEST=TRUE
103 37 28	IN	SOC_DFU_STATUS	FUNC_TEST=TRUE
38 30 29	IN	SOC_DOCK_CONNECT	FUNC_TEST=TRUE
103	IN	DFUMUX_SEL	FUNC_TEST=TRUE
103 28	IN	USB_SOC_TYPEC_P	FUNC_TEST=TRUE
103 28	IN	USB_SOC_TYPEC_N	FUNC_TEST=TRUE
103 28 12	IN	PCH_UART_DEBUG_R2D	FUNC_TEST=TRUE
103 28 12	IN	PCH_UART_DEBUG_D2R	FUNC_TEST=TRUE
103 38 15	IN	SWD_SOC_SWCLK	FUNC_TEST=TRUE
103 38 19	IN	SWD_SOC_SWDIO	FUNC_TEST=TRUE
103 38	IN	DEBUG_JTAG_SOC_TDI	FUNC_TEST=TRUE
103 38	IN	DEBUG_JTAG_SOC_TDO	FUNC_TEST=TRUE
38	IN	TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE
103 90 38	IN	SMC_DEBUGPRT_TX	FUNC_TEST=TRUE
103 90 38	IN	SMC_DEBUGPRT_RX	FUNC_TEST=TRUE
	IN	TP_SOC_DEBUGPRT_TX	FUNC_TEST=TRUE
103 98 39	IN	TP_SOC_DEBUGPRT_RX	FUNC_TEST=TRUE
50 38	IN	I2C_PWR_SCL	FUNC_TEST=TRUE
50 38	IN	I2C_PWR_SDA	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		4 TPs	

DFU/SOC/FCT DISCHARGE

100 31 28	IN	PP20V_USBC_XA_VBUS	FUNC_TEST=TRUE
100 31 28	IN	PP20V_USBC_XB_VBUS	FUNC_TEST=TRUE
100 93 90	IN	PP20V_USBC_TA_VBUS	FUNC_TEST=TRUE
100 93 90	IN	PP20V_USBC_TB_VBUS	FUNC_TEST=TRUE
100 97 67	IN	PPDCIN_G3H	FUNC_TEST=TRUE
100 67 66	IN	PPVBAT_G3H_CONN	FUNC_TEST=TRUE
100 97 67	IN	PPBUS_G3H	FUNC_TEST=TRUE
67	IN	PPDCIN_G3H_CHGR	FUNC_TEST=TRUE
67	IN	PPVBAT_G3H_CHGR_REG	FUNC_TEST=TRUE
	IN	SYS_DETECT	FUNC_TEST=TRUE
100 80 79	IN	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE

Memory Power

103 77 76	IN	PVDDQ_EN	FUNC_TEST=TRUE
77 76	IN	PVDDQ_PGOOD	FUNC_TEST=TRUE
100 97 77	IN	PP1V2_S3	FUNC_TEST=TRUE
97 8	IN	PP1V2_S3_CPUDDR	FUNC_TEST=TRUE
96 24 23 22 21	IN	PP1V8_S3_MEM	FUNC_TEST=TRUE
100 97 77	IN	PP0V6_S0_DDRVTT	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	

Wireless/BT Power

102 97 36 35	IN	PP3V3_G3S_WLANBT	FUNC_TEST=TRUE
97 36 35 34	IN	PP1V8_G3S_WLANBT_VDDIO	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	

Hall Effect

46	IN	LID_OPEN_LEFT	FUNC_TEST=TRUE
46	IN	LID_OPEN_RIGHT	FUNC_TEST=TRUE
100 64 49 46	IN	IPD_LID_OPEN	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		1 TPs	

DFU/SOC/FCT DMM/Power Sequence

100 97 67	IN	PPDCIN_G3H	FUNC_TEST=TRUE
100 67 66	IN	PPVBAT_G3H_CONN	FUNC_TEST=TRUE
100 97 67	IN	PPBUS_G3H	FUNC_TEST=TRUE
100 66	IN	SYS_DETECT_L	FUNC_TEST=TRUE
97 54 8	IN	PPVCC_S0_CPU	FUNC_TEST=TRUE
97 54 8	IN	PPVCCGT_S0_CPU	FUNC_TEST=TRUE
97 55 8	IN	PPVCCSA_S0_CPU	FUNC_TEST=TRUE
97 8 5	IN	PPVCCIO_S0_CPU	FUNC_TEST=TRUE
97 73	IN	PPVCCEDRAM_S0_CPU	FUNC_TEST=TRUE
96 75	IN	PP1V_S0SW	FUNC_TEST=TRUE 6 TPs
97 78	IN	PP1V2_S0SW	FUNC_TEST=TRUE
96 74	IN	PP1V_S3	FUNC_TEST=TRUE
96 74	IN	PP1V8_S3	FUNC_TEST=TRUE
100 97 77	IN	PP1V2_S3	FUNC_TEST=TRUE
100 97 77	IN	PP0V6_S0_DDRVTT	FUNC_TEST=TRUE
96 74	IN	PP1V_PRIM	FUNC_TEST=TRUE
96 74	IN	PPVPCORE_S5	FUNC_TEST=TRUE
96 75	IN	PP3V3_S5	FUNC_TEST=TRUE
96 74	IN	PP1V8_S5	FUNC_TEST=TRUE
96 14	IN	PP3V_G3H_RTC	FUNC_TEST=TRUE
102 100 80 50	IN	PP3V3_S0SW_LCD	FUNC_TEST=TRUE
102 100 97 80	IN	PP5V_S0SW_LCD	FUNC_TEST=TRUE
76 19	IN	ALL_SYS_PWRGD	FUNC_TEST=TRUE
76 19 15	IN	PCH_RTC_RESET_L	FUNC_TEST=TRUE
45 17 14	IN	PM_SYSRST_L	FUNC_TEST=TRUE
45 34 14	IN	PM_PCH_PWROK	FUNC_TEST=TRUE
45 14	IN	PM_PCH_SYS_PWROK	FUNC_TEST=TRUE
95 45 33 17 14	IN	PM_RSMRST_L	FUNC_TEST=TRUE
103 88 26 16 14 13	IN	PM_SLP_S3_L	FUNC_TEST=TRUE
103 76 38 19	IN	PM_SLP_S0_L	FUNC_TEST=TRUE
45 19 16 14	IN	PLT_RST_L	FUNC_TEST=TRUE
76 45 6	IN	PM_THRMTRIP_L	FUNC_TEST=TRUE
76 17 14	IN	PCH_PWRBTN_L	FUNC_TEST=TRUE
6	IN	CPU_PROCHOT_R_L	FUNC_TEST=TRUE
76 6	IN	CPU_CATERR_L	FUNC_TEST=TRUE
68	IN	CPU_VR_READY	FUNC_TEST=TRUE
103 96 74	IN	PP1V8_SLPS2R	FUNC_TEST=TRUE
103 96 74	IN	PP1V8_AWAKE	FUNC_TEST=TRUE
96 74	IN	PP1V1_SLPS2R	FUNC_TEST=TRUE
96 75	IN	PP0V8_SLPS2R	FUNC_TEST=TRUE
96 74	IN	PP0V82_SLPDDR	FUNC_TEST=TRUE
96 75	IN	PP3V3_AWAKE	FUNC_TEST=TRUE
96 74	IN	PPVDDCPUSRAM_AWAKE	FUNC_TEST=TRUE
96 74	IN	PP0V9_SLPDDR	FUNC_TEST=TRUE
96 75	IN	PP1V1_SLPDDR	FUNC_TEST=TRUE
96 75	IN	PP1V2_AWAKE	FUNC_TEST=TRUE
96 74	IN	PPVDDCPU_AWAKE	FUNC_TEST=TRUE
76 63 38	IN	PMU_COLD_RESET_L	FUNC_TEST=TRUE
85 76 38 37	IN	PMU_SYS_ALIVE	FUNC_TEST=TRUE
103 76 37 29	IN	PMU_ACTIVE_READY	FUNC_TEST=TRUE
67 66	IN	CHGR_EN_MVR	FUNC_TEST=TRUE
97 66	IN	PP3V3_G3H_RTC	FUNC_TEST=TRUE
76 72	IN	PMU_PVDDMAIN_EN	FUNC_TEST=TRUE
97 72	IN	PP3V3_G3H	FUNC_TEST=TRUE
98 38	IN	TP_SMC_FIXTURE_MODE_L	FUNC_TEST=TRUE
76 38	IN	SOC_WDOG	FUNC_TEST=TRUE
103 76 37	IN	SOC_SOCHOT_L	FUNC_TEST=TRUE
90 76 66 28	IN	UPC_PMU_RESET	FUNC_TEST=TRUE
100 47	IN	PMU_ONOFF_R_L_CONN	FUNC_TEST=TRUE
78 76	IN	P3V3G3S_EN	FUNC_TEST=TRUE
97 78	IN	PP3V3_G3S	FUNC_TEST=TRUE
76 72	IN	P5VG3S_EN	FUNC_TEST=TRUE
97 72	IN	PP5V_G3S	FUNC_TEST=TRUE
103 78 76	IN	P1V8G3S_EN	FUNC_TEST=TRUE
97 78	IN	PP1V8_G3S	FUNC_TEST=TRUE
85 46 37	IN	SSD_PMU_RESET_L	FUNC_TEST=TRUE
86 85 84 83 82 81	IN	PP1V8_SSD0	FUNC_TEST=TRUE
85 84 83 82 81	IN	PP0V9_SSD0	FUNC_TEST=TRUE
85 84 83 82 81	IN	PP2V7_NAND_SSD0	FUNC_TEST=TRUE
85 84 83 82 81	IN	SSD0_OCARINA_WP_L	FUNC_TEST=TRUE
85 84 83 82 81	IN	SSD0_OCARINA_PFN	FUNC_TEST=TRUE
85 84 83 82 81	IN	SSD0_OCARINA_RESET_L	FUNC_TEST=TRUE

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DP_DDI1_ML_C_N<0>	PP9901	MIPI_FTCAM_DATA_P<0>	PP9949
DP_DDI1_ML_C_P<0>	PP9902	MIPI_FTCAM_DATA_N<0>	PP9950
DP_DDI2_ML_C_N<0>	PP9903	MIPI_FTCAM_CLK_P	PP9951
DP_DDI2_ML_C_P<0>	PP9904	MIPI_FTCAM_CLK_N	PP9952
PCIE_SSD0_D2R_N<0>	PP9910	MIPI_DFR_DATA_FILT_CONN_P	
PCIE_SSD0_D2R_P<0>	PP9911	MIPI_DFR_DATA_FILT_CONN_N	
PCIE_TBT_X_D2R_N<0>	PP9919	MIPI_DFR_CLK_FILT_CONN_P	
PCIE_TBT_X_D2R_P<0>	PP9920	MIPI_DFR_CLK_FILT_CONN_N	
PCIE_TBT_T_D2R_N<0>	PP9927	MIPI_FTCAM_DATA_ISOL_FILT_CONN_P<0>	
PCIE_TBT_T_D2R_P<0>	PP9928	MIPI_FTCAM_DATA_ISOL_FILT_CONN_N<0>	
PCIE_CLK100M_SOC_N	PP9939	MIPI_FTCAM_CLK_ISOL_FILT_CONN_P	
PCIE_CLK100M_SOC_P	PP9940	MIPI_FTCAM_CLK_ISOL_FILT_CONN_N	
PCIE_CLK100M_SSD0_01_N	PP9941		
PCIE_CLK100M_SSD0_01_P	PP9942		
PCIE_CLK100M_SSD0_23_N	PP9953		
PCIE_CLK100M_SSD0_23_P	PP9954		
PCIE_CLK100M_TBT_X_N	PP9943		
PCIE_CLK100M_TBT_X_P	PP9944		
PCIE_CLK100M_TBT_T_N	PP9945		
PCIE_CLK100M_TBT_T_P	PP9946		
PCH_PCIE_CLK100M_WLAN_N	PP9947		
PCH_PCIE_CLK100M_WLAN_P	PP9948		
XDP_USB_EXTA_OC_L	PP9801		
XDP_USB_EXTB_OC_L	PP9802		
XDP_USB_EXTC_OC_L	PP9803		
XDP_USB_EXTD_OC_L	PP9804		
XDP_BPM_L<0>	TP9820		

SAR Fusion Sensor Debug

SPI_ACCEL_CS_L	PP9961
SPI_AOP_SENSOR_CLK	PP9962
SPI_AOP_SENSOR_MOSI	PP9963
SPI_AOP_SENSOR_MISO	PP9964
ACCEL_INT1	PP9965

AUDIO CODEC

I2S_CODEC_BCLK	PP9966
I2S_CODEC_LRCLK_R	PP9967
I2S_CODEC_R2D	PP9968

AUDIO SPKRAMP

I2S_SPKRAMP_R_LRCLK_R	PP9969

SOC SENSE

SOC_VDDCPU_SENSE	PP9930

ACE-TR AUX/LS

USBC_XA_AUXLSX1	PP9970
USBC_XA_AUXLSX2	PP9971
USBC_XB_AUXLSX1	PP9972
USBC_XB_AUXLSX2	PP9973
USBC_TA_AUXLSX1	PP9974
USBC_TA_AUXLSX2	PP9975
USBC_TB_AUXLSX1	PP9976
USBC_TB_AUXLSX2	PP9977

ACE GPIO PPs

UPC_XA_GPIO0	PP9978
UPC_XB_GPIO0	PP9979
UPC_TA_GPIO0	PP9980
UPC_TA_GPIO1	PP9981

SoC PPs

TEST_SOC_AMUXOUT	PP9990
TEST_SOC_TST_CLKOUT	PP9991

WIRELESS PPs

WLAN_CONTEXT_A	PP9994
WLAN_CONTEXT_B	PP9995

PMIC Switch Nodes

PVDDCPUAWAKE_SW0	PP7806
PVDDCPUAWAKE_SW1	PP7807
PVDDCPUAWAKE_SW2	PP7808
PVDDCPUAWAKE_SW3	PP7809
PVDDCPUSRAMAWAKE_SW0	PP7810
P0V8SLPDDR_SW0	PP7811
P0V8SLPDDR_SW1	PP7812
P1V8SLPS2R_SW0	PP7813
P1V1SLPS2R_SW0	PP7814
P1V1SLPS2R_SW1	PP7815
P0V9SLPDDR_SW0	PP7816
P0V9SLPDDR_SW1	PP7817
PVCCPCOREPRIM_SW0	PP7819
PVCCPCOREPRIM_SW1	PP7820
P1VPRIM_SW0	PP7821
P1VPRIM_SW1	PP7822

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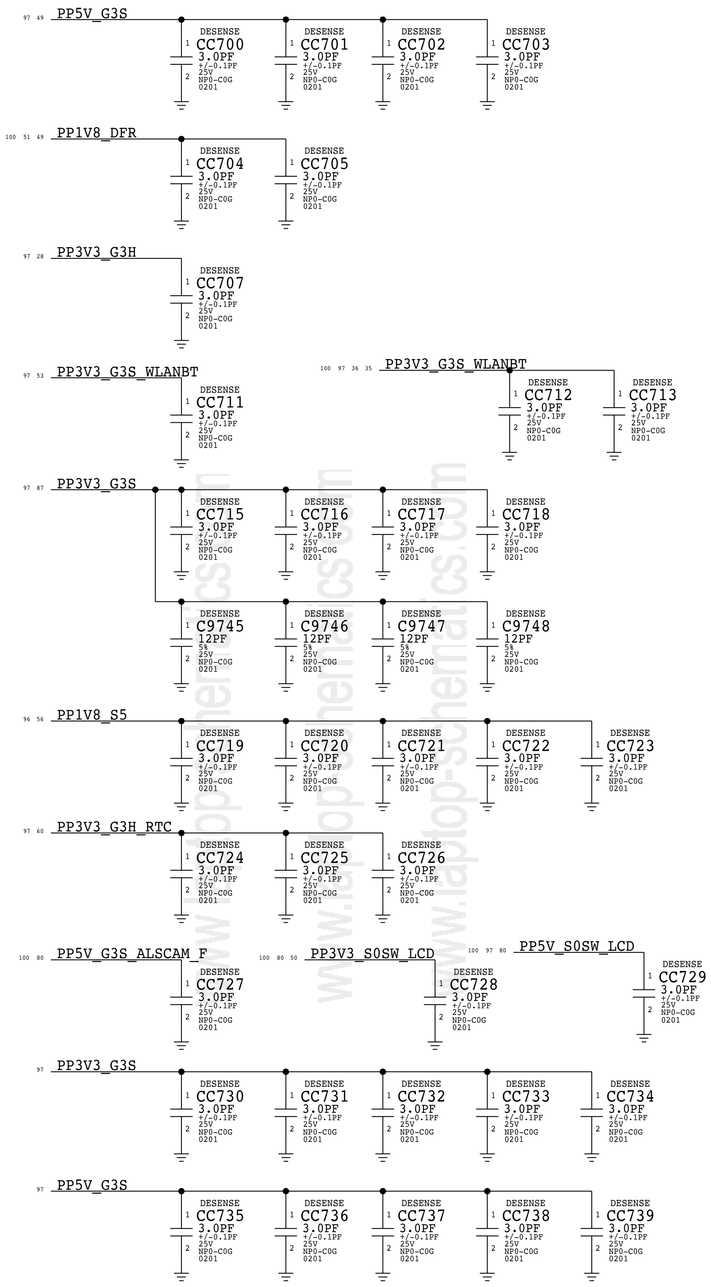

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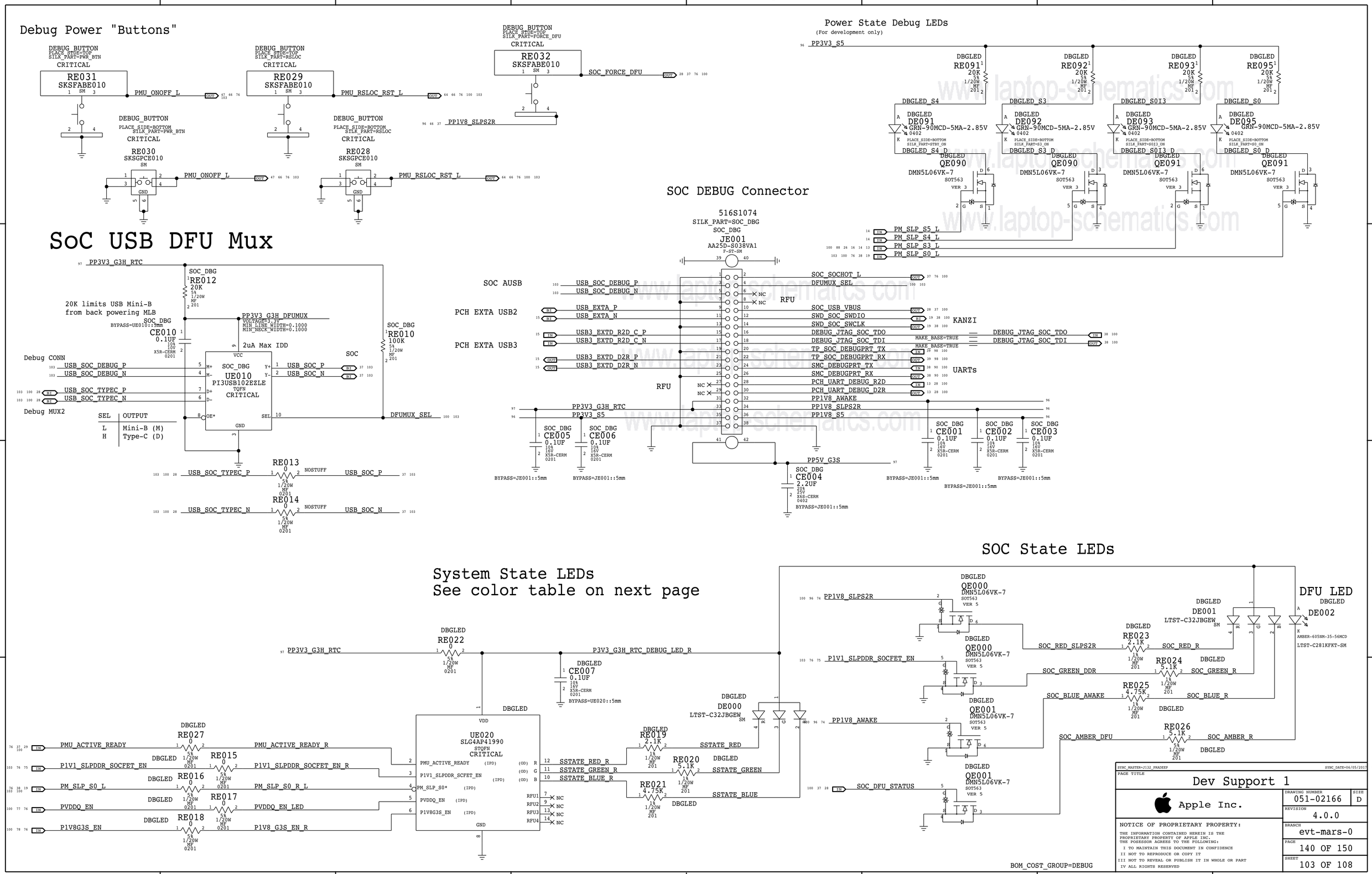
Debug Power "Buttons"
DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=PWR_BTN
CRITICAL
RE031
SKSFABE010
PMU_ONOFF_L
DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=PWR_BTN
CRITICAL
RE030
SKSGPCE010
PMU_ONOFF_L
DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=RSLOC
CRITICAL
RE029
SKSFABE010
PMU_RSLOC_RST_L
DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=RSLOC
CRITICAL
RE028
SKSGPCE010
PMU_RSLOC_RST_L
DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=FORCE_DFU
CRITICAL
RE032
SKSFABE010
SOC_FORCE_DFU
PP1V8_SLPS2R
Power State Debug LEDs
(For development only)
PP3V3_S5
DBGLED
RE091
RE092
RE093
RE095
20K
DBGLED_S4
DBGLED_S3
DBGLED_SOI3
DBGLED_S0
DBGLED
DE091
DE092
DE093
DE095
GRN-90MCD-5MA-2.85V
DBGLED_S4_D
DBGLED_S3_D
DBGLED_SOI3_D
DBGLED_S0_D
DBGLED
QE090
QE091
DMN5L06VK-7
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_S0_L
SoC USB DFU Mux
PP3V3_G3H_RTC
SOC_DBG
RE012
20K
20K limits USB Mini-B
from back powering MLB
PP3V3_G3H_DFUMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
CE010
0.1UF
2uA Max IDD
RE010
100K
Debug CONN
USB_SOC_DEBUG_P
USB_SOC_DEBUG_N
USB_SOC_TYPEC_P
USB_SOC_TYPEC_N
UE010
PI3USB102EZLE
TQFN
CRITICAL
SOC
DFUMUX_SEL
Debug MUX2
SEL | OUTPUT
L | Mini-B (M)
H | Type-C (D)
RE013
RE014
NOSTUFF
USB_SOC_P
USB_SOC_N
SOC DEBUG Connector
516S1074
SILK_PART=SOC_DBG
SOC_DBG
JE001
AA25D-S038VA1
SOC AUSB
USB_SOC_DEBUG_P
USB_SOC_DEBUG_N
PCH EXTA USB2
USB_EXTA_P
USB_EXTA_N
PCH EXTA USB3
USB3_EXTD_R2D_C_P
USB3_EXTD_R2D_C_N
USB3_EXTD_D2R_P
USB3_EXTD_D2R_N
RFU
SOC_SOCHOT_L
DFUMUX_SEL
SOC_USB_VBUS
SWD_SOC_SWDIO
SWD_SOC_SWCLK
DEBUG_JTAG_SOC_TDO
DEBUG_JTAG_SOC_TDI
TP_SOC_DEBUGPRT_TX
TP_SOC_DEBUGPRT_RX
SMC_DEBUGPRT_TX
SMC_DEBUGPRT_RX
PCH_UART_DEBUG_R2D
PCH_UART_DEBUG_D2R
PP1V8_AWAKE
PP1V8_SLPS2R
PP1V8_S5
KANZI
DEBUG_JTAG_SOC_TDO
DEBUG_JTAG_SOC_TDI
UARTs
PP3V3_G3H_RTC
PP3V3_S5
PP5V_G3S
CE005
CE006
CE001
CE002
CE003
CE004
2.2UF
BYPASS=JE001::5mm
System State LEDs
See color table on next page
DBGLED
RE022
P3V3_G3H_RTC_DEBUG_LED_R
CE007
0.1UF
BYPASS=UE020::5mm
UE020
SLG4AP41990
STQFN
CRITICAL
PMU_ACTIVE_READY
P1V1_SLPDDR_SOCFET_EN
PM_SLP_S0*
PVDDQ_EN
P1V8G3S_EN
PMU_ACTIVE_READY_R
P1V1_SLPDDR_SOCFET_EN_R
PM_SLP_S0_R_L
PVDDQ_EN_LED
P1V8_G3S_EN_R
RE027
RE015
RE016
RE017
RE018
SSTATE_RED_R
SSTATE_GREEN_R
SSTATE_BLUE_R
RE019
RE020
RE021
SSTATE_RED
SSTATE_GREEN
SSTATE_BLUE
DE000
LTST-C32JBGEW
SOC State LEDs
QE000
QE001
PP1V8_SLPS2R
P1V1_SLPDDR_SOCFET_EN
PP1V8_AWAKE
SOC_DFU_STATUS
SOC_RED_SLPS2R
SOC_GREEN_DDR
SOC_BLUE_AWAKE
SOC_AMBER_DFU
RE023
RE024
RE025
RE026
SOC_RED_R
SOC_GREEN_R
SOC_BLUE_R
SOC_AMBER_R
DFU LED
DE001
DE002
LTST-C32JBGEW
AMBER-605NM-35-56MCD
LTST-C281KFKT-SM
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SYNC_DATE=06/05/2017
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UE020 SAK Truth Table:

INPUTS					OUTPUTS (OD)			
PMU_ACT_RDY	SLP_SCFET_EN	SLP_S0_L	VDDQ_EN	1V8G3S_EN	R	G	B	COLOR
0	0	0	0	0	BLINK	1	1	Blinking Red
0	0	0	0	1	0	1	1	Red
0	0	0	1	0	0	1	0	Magenta
0	0	0	1	1	0	0	0	White
0	0	1	0	0	0	1	0	Magenta
0	0	1	0	1	0	1	0	Magenta
0	0	1	1	0	0	1	0	Magenta
0	0	1	1	1	0	1	0	Magenta
0	1	0	0	0	0	1	0	Magenta
0	1	0	0	1	0	1	0	Magenta
0	1	0	1	0	0	1	0	Magenta
0	1	0	1	1	0	1	0	Magenta
0	1	1	0	0	0	1	0	Magenta
0	1	1	0	1	0	1	0	Magenta
0	1	1	1	0	0	1	0	Magenta
0	1	1	1	1	0	1	0	Magenta
1	0	0	0	0	0	1	0	Magenta
1	0	0	0	1	0	1	0	Magenta
1	0	0	1	0	0	1	0	Magenta
1	0	0	1	1	0	1	0	Magenta
1	0	1	0	0	0	1	0	Magenta
1	0	1	0	1	0	1	0	Magenta
1	0	1	1	0	0	1	0	Magenta
1	0	1	1	1	0	1	0	Magenta
1	1	0	0	0	BLINK	0	1	Blinking Green & Yellow
1	1	0	0	1	0	0	1	Yellow
1	1	0	1	0	0	1	0	Magenta
1	1	0	1	1	1	1	0	Blue
1	1	1	0	0	0	1	0	Magenta
1	1	1	0	1	0	1	0	Magenta
1	1	1	1	0	0	1	0	Magenta
1	1	1	1	1	1	0	1	Green

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Dev Support 2

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00187	COMMON PARTS,MLB,X941	X941_COMMON
985-00366	DEV,MLB,X941	X941_DEVEL:ENG
939-05022	PCBA,MLB,NO CPU,SS-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,DRAMCFG:SS_8G,NANDCFG:SD_256G
939-05023	PCBA,MLB,CPU SOCKET,SS-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:SOCKET,DRAMCFG:SS_8G,NANDCFG:SD_256G
939-05373	PCBA,MLB,2.3G,HY-8G,SS-2T-DOE,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:SS_2T_DOE
939-05374	PCBA,MLB,2.3G,MI-8G,SD-256G-DOE,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:SD_256G_DOE
939-05375	PCBA,MLB,2.3G,SS-8G,TO-256G-DOE,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:TO_256G_DOE
939-05698	PCBA,MLB,NO CPU,RF DOE,X941	SCH,PCB,RF_DOE

BOM NUMBER	BOM NAME	BOM OPTIONS
639-05125	PCBA,MLB,2.3G,HY-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:SD_256G
639-05126	PCBA,MLB,2.3G,HY-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:TO_256G
639-05127	PCBA,MLB,2.3G,MI-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:SD_256G
639-05128	PCBA,MLB,2.3G,MI-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:TO_256G
639-05129	PCBA,MLB,2.3G,SS-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:SD_256G
639-05130	PCBA,MLB,2.3G,SS-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:TO_256G
639-05131	PCBA,MLB,2.3G,HY-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:SD_256G
639-05132	PCBA,MLB,2.3G,HY-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:TO_256G
639-05133	PCBA,MLB,2.3G,MI-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:SD_256G
639-05134	PCBA,MLB,2.3G,MI-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:TO_256G
639-05135	PCBA,MLB,2.3G,SS-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:SD_256G
639-05136	PCBA,MLB,2.3G,SS-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:TO_256G
639-05193	PCBA,MLB,2.3G,HY-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:SD_512G
639-05194	PCBA,MLB,2.3G,HY-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:TO_512G
639-05195	PCBA,MLB,2.3G,MI-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:SD_512G
639-05196	PCBA,MLB,2.3G,MI-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:TO_512G
639-05197	PCBA,MLB,2.3G,SS-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:SD_512G
639-05198	PCBA,MLB,2.3G,SS-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:TO_512G
639-05199	PCBA,MLB,2.3G,HY-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:SD_512G
639-05200	PCBA,MLB,2.3G,HY-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:TO_512G
639-05201	PCBA,MLB,2.3G,MI-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:SD_512G
639-05202	PCBA,MLB,2.3G,MI-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:TO_512G
639-05203	PCBA,MLB,2.3G,SS-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:SD_512G
639-05204	PCBA,MLB,2.3G,SS-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:TO_512G
639-05205	PCBA,MLB,2.3G,HY-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:SD_1T
639-05206	PCBA,MLB,2.3G,HY-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:SS_1T
639-05207	PCBA,MLB,2.3G,HY-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:TO_1T
639-05208	PCBA,MLB,2.3G,MI-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:SD_1T
639-05209	PCBA,MLB,2.3G,MI-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:SS_1T
639-05210	PCBA,MLB,2.3G,MI-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:TO_1T
639-05211	PCBA,MLB,2.3G,SS-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:SD_1T
639-05212	PCBA,MLB,2.3G,SS-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:SS_1T
639-05213	PCBA,MLB,2.3G,SS-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:TO_1T
639-05214	PCBA,MLB,2.3G,HY-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:SD_1T
639-05215	PCBA,MLB,2.3G,HY-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:SS_1T
639-05216	PCBA,MLB,2.3G,HY-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:TO_1T
639-05217	PCBA,MLB,2.3G,MI-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:SD_1T
639-05218	PCBA,MLB,2.3G,MI-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:SS_1T
639-05219	PCBA,MLB,2.3G,MI-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:TO_1T
639-05220	PCBA,MLB,2.3G,SS-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:SD_1T
639-05221	PCBA,MLB,2.3G,SS-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:SS_1T
639-05222	PCBA,MLB,2.3G,SS-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:TO_1T
639-05223	PCBA,MLB,2.3G,HY-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_8G,NANDCFG:SS_2T
639-05224	PCBA,MLB,2.3G,MI-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_8G,NANDCFG:SS_2T
639-05225	PCBA,MLB,2.3G,SS-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_8G,NANDCFG:SS_2T
639-05226	PCBA,MLB,2.3G,HY-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:HY_16G,NANDCFG:SS_2T
639-05227	PCBA,MLB,2.3G,MI-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:MI_16G,NANDCFG:SS_2T
639-05228	PCBA,MLB,2.3G,SS-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.3G,DRAMCFG:SS_16G,NANDCFG:SS_2T

BOM NUMBER	BOM NAME	BOM OPTIONS
639-05528	PCBA,MLB,2.5G,HY-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:SD_256G
639-05529	PCBA,MLB,2.5G,HY-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:TO_256G
639-05530	PCBA,MLB,2.5G,MI-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:SD_256G
639-05531	PCBA,MLB,2.5G,MI-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:TO_256G
639-05532	PCBA,MLB,2.5G,SS-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:SD_256G
639-05533	PCBA,MLB,2.5G,SS-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:TO_256G
639-05534	PCBA,MLB,2.5G,HY-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:SD_256G
639-05535	PCBA,MLB,2.5G,HY-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:TO_256G
639-05536	PCBA,MLB,2.5G,MI-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:SD_256G
639-05537	PCBA,MLB,2.5G,MI-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:TO_256G
639-05538	PCBA,MLB,2.5G,SS-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:SD_256G
639-05539	PCBA,MLB,2.5G,SS-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:TO_256G
639-05540	PCBA,MLB,2.5G,HY-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:SD_512G
639-05541	PCBA,MLB,2.5G,HY-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:TO_512G
639-05542	PCBA,MLB,2.5G,MI-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:SD_512G
639-05543	PCBA,MLB,2.5G,MI-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:TO_512G
639-05544	PCBA,MLB,2.5G,SS-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:SD_512G
639-05545	PCBA,MLB,2.5G,SS-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:TO_512G
639-05546	PCBA,MLB,2.5G,HY-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:SD_512G
639-05547	PCBA,MLB,2.5G,HY-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:TO_512G
639-05548	PCBA,MLB,2.5G,MI-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:SD_512G
639-05549	PCBA,MLB,2.5G,MI-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:TO_512G
639-05550	PCBA,MLB,2.5G,SS-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:SD_512G
639-05551	PCBA,MLB,2.5G,SS-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:TO_512G
639-05552	PCBA,MLB,2.5G,HY-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:SD_1T
639-05553	PCBA,MLB,2.5G,HY-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:SS_1T
639-05554	PCBA,MLB,2.5G,HY-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:TO_1T
639-05555	PCBA,MLB,2.5G,MI-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:SD_1T
639-05556	PCBA,MLB,2.5G,MI-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:SS_1T
639-05557	PCBA,MLB,2.5G,MI-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:TO_1T
639-05558	PCBA,MLB,2.5G,SS-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:SD_1T
639-05559	PCBA,MLB,2.5G,SS-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:SS_1T
639-05560	PCBA,MLB,2.5G,SS-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:TO_1T
639-05561	PCBA,MLB,2.5G,HY-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:SD_1T
639-05562	PCBA,MLB,2.5G,HY-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:SS_1T
639-05563	PCBA,MLB,2.5G,HY-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:TO_1T
639-05564	PCBA,MLB,2.5G,MI-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:SD_1T
639-05565	PCBA,MLB,2.5G,MI-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:SS_1T
639-05566	PCBA,MLB,2.5G,MI-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:TO_1T
639-05567	PCBA,MLB,2.5G,SS-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:SD_1T
639-05568	PCBA,MLB,2.5G,SS-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:SS_1T
639-05569	PCBA,MLB,2.5G,SS-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:TO_1T
639-05570	PCBA,MLB,2.5G,HY-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_8G,NANDCFG:SS_2T
639-05571	PCBA,MLB,2.5G,MI-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_8G,NANDCFG:SS_2T
639-05572	PCBA,MLB,2.5G,SS-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_8G,NANDCFG:SS_2T
639-05573	PCBA,MLB,2.5G,HY-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:HY_16G,NANDCFG:SS_2T
639-05574	PCBA,MLB,2.5G,MI-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:MI_16G,NANDCFG:SS_2T
639-05575	PCBA,MLB,2.5G,SS-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.5G,DRAMCFG:SS_16G,NANDCFG:SS_2T

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BOM Variants 1

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-05576	PCBA,MLB,2.6G,HY-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SD_256G
639-05577	PCBA,MLB,2.6G,HY-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:TO_256G
639-05578	PCBA,MLB,2.6G,MI-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SD_256G
639-05579	PCBA,MLB,2.6G,MI-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:TO_256G
639-05580	PCBA,MLB,2.6G,SS-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SD_256G
639-05581	PCBA,MLB,2.6G,SS-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:TO_256G
639-05582	PCBA,MLB,2.6G,HY-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SD_256G
639-05583	PCBA,MLB,2.6G,HY-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:TO_256G
639-05584	PCBA,MLB,2.6G,MI-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SD_256G
639-05585	PCBA,MLB,2.6G,MI-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:TO_256G
639-05586	PCBA,MLB,2.6G,SS-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SD_256G
639-05587	PCBA,MLB,2.6G,SS-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:TO_256G
639-05588	PCBA,MLB,2.6G,HY-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SD_512G
639-05589	PCBA,MLB,2.6G,HY-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:TO_512G
639-05590	PCBA,MLB,2.6G,MI-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SD_512G
639-05591	PCBA,MLB,2.6G,MI-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:TO_512G
639-05592	PCBA,MLB,2.6G,SS-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SD_512G
639-05593	PCBA,MLB,2.6G,SS-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:TO_512G
639-05594	PCBA,MLB,2.6G,HY-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SD_512G
639-05595	PCBA,MLB,2.6G,HY-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:TO_512G
639-05596	PCBA,MLB,2.6G,MI-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SD_512G
639-05597	PCBA,MLB,2.6G,MI-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:TO_512G
639-05598	PCBA,MLB,2.6G,SS-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SD_512G
639-05599	PCBA,MLB,2.6G,SS-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:TO_512G
639-05600	PCBA,MLB,2.6G,HY-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SD_1T
639-05601	PCBA,MLB,2.6G,HY-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SS_1T
639-05602	PCBA,MLB,2.6G,HY-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:TO_1T
639-05603	PCBA,MLB,2.6G,MI-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SD_1T
639-05604	PCBA,MLB,2.6G,MI-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SS_1T
639-05605	PCBA,MLB,2.6G,MI-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:TO_1T
639-05606	PCBA,MLB,2.6G,SS-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SD_1T
639-05607	PCBA,MLB,2.6G,SS-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SS_1T
639-05608	PCBA,MLB,2.6G,SS-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:TO_1T
639-05609	PCBA,MLB,2.6G,HY-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SD_1T
639-05610	PCBA,MLB,2.6G,HY-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SS_1T
639-05611	PCBA,MLB,2.6G,HY-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:TO_1T
639-05612	PCBA,MLB,2.6G,MI-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SD_1T
639-05613	PCBA,MLB,2.6G,MI-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SS_1T
639-05614	PCBA,MLB,2.6G,MI-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:TO_1T
639-05615	PCBA,MLB,2.6G,SS-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SD_1T
639-05616	PCBA,MLB,2.6G,SS-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SS_1T
639-05617	PCBA,MLB,2.6G,SS-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:TO_1T
639-05618	PCBA,MLB,2.6G,HY-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SS_2T
639-05619	PCBA,MLB,2.6G,MI-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SS_2T
639-05620	PCBA,MLB,2.6G,SS-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SS_2T
639-05621	PCBA,MLB,2.6G,HY-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SS_2T
639-05622	PCBA,MLB,2.6G,MI-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SS_2T
639-05623	PCBA,MLB,2.6G,SS-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SS_2T

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Alternate Parts

System EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
103S0321	103S0276		ALL	
103S00248	103S00247		ALL	8.06K 0.1% RESISTOR
103S00250	103S00249		ALL	18.2K 0.1% RESISTOR
107S0284	107S00021	SENSOR:DEV	ALL	TFT w/ Yageo
107S00101	107S00005	SENSOR:DEV	ALL	Cyntec w/ Yageo
107S00102	107S00017	SENSOR:DEV	ALL	Cyntec w/ Yageo
107S0276	107S00020	SENSOR:DEV	ALL	Cyntec w/ TFT
107S00086	107S00056	ANY	ALL	TFT w/ Cyntec
107S00100	107S00057		ALL	Cyntec w/ TFT
107S00103	107S00058	SENSOR:DEV	ALL	Cyntec w/ Yageo
107S00070	107S0085		ALL	100K THERMISTOR
132S00202	132S00175		ALL	
138S00084	138S00060		ALL	
138S00117	138S00071		ALL	
138S0714	138S0713		ALL	Murata w/ Samsung
138S0715	138S0732		ALL	Murata w/ Samsung
138S0706	138S0739		ALL	NEC w/ Vishay
138S0945	138S0739		ALL	NEC w/ Rohm
138S00049	138S0831	ANY	ALL	
138S00006	138S0835		ALL	
138S00086	138S0884		ALL	
138S00104	138S0978		ALL	Murata w/ Taiyo
138S00056	138S1100		ALL	
152S00369	152S00268		ALL	Cyntec w/ NEC
152S00403	152S00322		ALL	Murata w/ Chillisin
152S00864	152S00851		ALL	
152S00434	152S1829		ALL	
155S0665	155S00232		ALL	
155S00166	155S0391		ALL	
155S00018	155S0664		ALL	Murata w/ Taiyo
155S00007	155S0667		ALL	
155S0914	155S0897		ALL	
155S00190	155S0897		ALL	
197S00046	197S00036		ALL	Epson w/ TXC
197S00047	197S00036		ALL	Kyocera w/ TXC
197S00048	197S00036		ALL	Murata w/ TXC
197S00053	197S00050		ALL	Kyocera w/ TXC
197S00054	197S00050		ALL	NDK w/ TXC
197S00055	197S00050		ALL	Murata w/ TXC
197S00120	197S00118		ALL	
311S0426	311S00007		ALL	
311S00104	311S00091	ANY	ALL	
311S00156	311S00129		ALL	
311S00196	311S00195		ALL	
311S00060	311S0273		ALL	
311S00121	311S0398		ALL	
311S00138	311S0436		ALL	
311S00013	311S0508		ALL	NXP w/ Diodes
335S00270	335S00203		ALL	
335S00213	335S0888		ALL	
353S00878	353S00599		ALL	
353S00879	353S00754		ALL	
353S00750	353S00877		ALL	
353S01041	353S01042		ALL	
353S01346	353S01320		ALL	
353S01506	353S01404	ANY	ALL	
353S00107	353S3239	ANY	ALL	Onsemi alt to Intersil
353S00636	353S4037	ANY	ALL	
353S00772	353S4068		ALL	
371S00089	371S00085		ALL	

System EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S00170	371S00125		ALL	
371S00127	371S00182		ALL	
372S00016	372S00015		ALL	
372S0186	372S0185		ALL	
376S00219	376S00079		ALL	
376S00292	376S00294		ALL	
376S1080	376S0820		ALL	
376S00074	376S0855		ALL	
376S00146	376S1061		ALL	NXP w/ Diodes
376S00282	376S1128		ALL	
377S00079	377S00077		ALL	
377S0077	377S0183		ALL	Infineon w/ ST
740S00033	740S00002		ALL	
740S00019	740S00007		ALL	Bourns w/ Polytronics
740S00003	740S0135		ALL	

Audio

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0700	138S0641		ALL	Murata w/ SS&Taiyo
138S0660	138S0684		ALL	
138S0689	138S0701		ALL	
138S1103	138S0719		ALL	
155S0694	155S0387		ALL	
155S0660	155S0513		ALL	
155S00034	155S0706		ALL	Taiyo w/ Murata
155S00203	155S0894		ALL	
311S0271	311S00008		ALL	

BLC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S00033	107S00034		ALL	
138S0738	138S1101		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
152S00359	152S00253		ALL	Chilisin alt to Cyntec
353S01615	353S4160		ALL	Aizu alt to Maine
371S00180	371S00077		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1106	376S0678		ALL	Fairchild alt to Vishay
740S00041	740S0159		ALL	

WIRELESS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00024	138S0986		ALL	
152S00769	152S00659		ALL	
152S00770	152S0857		ALL	
155S00067	155S00401		ALL	
339S00428	339S00458		ALL	

DC-DC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S00015	107S00011		ALL	
107S00087	107S00029		ALL	TFT w/ Yageo
107S00071	107S00053		ALL	
107S00139	107S0178		ALL	
107S0249	107S0251		ALL	
128S00009	128S00007		ALL	
128S00070	128S00007		ALL	
128S00026	128S00011		ALL	
128S00031	128S00011		ALL	
128S00087	128S00011		ALL	
128S0302	128S00038		ALL	
128S00039	128S00038		ALL	
128S00062	128S00067		ALL	
128S00065	128S00067		ALL	
128S00069	128S00067		ALL	
128S0364	128S0264		ALL	Kemet w/ Panasonic
128S0578	128S0351		ALL	
128S00050	128S0351		ALL	
132S00012	132S0401		ALL	
132S00064	132S0409		ALL	
138S00077	138S00035		ALL	
138S00093	138S00035		ALL	
138S00111	138S00036		ALL	
138S00047	138S00073		ALL	
138S00229	138S00107		ALL	
138S0786	138S0705		ALL	Murata w/ Samsung
138S00097	138S0750		ALL	
138S0863	138S0853		ALL	
138S0775	138S0860		ALL	
138S0789	138S0941		ALL	Murata w/ SS
152S00363	152S00048		ALL	Cyntec w/ Vishay
152S00388	152S00182		ALL	
152S00703	152S00182		ALL	
152S00383	152S00198		ALL	
152S00680	152S00198		ALL	
152S00398	152S00204		ALL	
152S00841	152S00238		ALL	
152S00765	152S00239		ALL	
152S00368	152S00269		ALL	
152S00724	152S00311		ALL	
152S00786	152S00344		ALL	
152S00725	152S00590		ALL	
152S00726	152S00592		ALL	
152S00707	152S00689		ALL	
311S0596	311S0593		ALL	NXP w/ Diodes
311S00192	311S00191		ALL	
311S00193	311S00191		ALL	
353S00831	353S00519		ALL	
353S00796	353S00497		ALL	
353S00832	353S00525		ALL	
376S00303	376S00012		ALL	
376S00204	376S00203		ALL	
376S00226	376S00203		ALL	
376S00227	376S00203		ALL	
376S00302	376S1038		ALL	
376S00281	376S1147		ALL	
376S00007	376S1179		ALL	
376S00228	376S1179		ALL	
376S00304	376S1187		ALL	
740S0144	740S0118		ALL	
740S00028	740S0118		ALL	

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